ES 210 – Spring 2016

Course Name: Digital Circuits and Logic Design, ES 210
Instructor: Loren Betts
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Course page: https://canvas.instructure.com/courses/991766

Class Schedule (Salazar 2009A): Tuesday: 1:00pm to 2:15pm (lecture), 2:15pm to 5:00pm (lab - Salazar 2005) and Thursday: 1:00pm to 2:15pm (lecture).

Office Hours (Salazar 2008A): Tuesday: 2:15pm to 3:00pm and Thursday: 2:15pm to 3:00pm.


Assignments: On the day that the assignment is due, please bring the completed problems with you. Assignments are due at the beginning of lecture and no late assignments will be accepted. Please show all work!

Labs: There will be one lab per week with lab homework. In the lab you will be using the principles learned in class to program digital logic in the Verilog language as well as design digital hardware circuits. Take home lab homework is due at the beginning of the lab.

Exams: There will be one mid-term exam and one final exam. See the Canvas schedule of homework assignments for the due dates and the chapters covered for each exam.

Canvas: I am not normally located on campus, so Canvas will be a great resource for this class. I will post homework assignments, homework solutions, lecture notes, calendar information, and additional resources on this website. It is required that you use Canvas. It will be the primarily location for class announcements, schedule changes, etc. If you have not received an invitation from me, please let me know immediately.

Grade:

<table>
<thead>
<tr>
<th>Category</th>
<th>Percentage</th>
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</thead>
<tbody>
<tr>
<td>Assignments</td>
<td>15%</td>
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<tr>
<td>Labs</td>
<td>25%</td>
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<tr>
<td>Mid-term Exam</td>
<td>30%</td>
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<tr>
<td>Final exam</td>
<td>30% (The final will cover all topics)</td>
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Class Outline: Here is a rough outline of the units we will be covering. These are subject to change. Approximately 28 lectures.

1. Binary Numbers (Chapter 1) - 3 lectures
2. Boolean Algebra and Logic Gates (Chapter 2) - 3 lectures
3. Gate Level Minimization (Chapter 3) - 4 lectures
4. Combinational Logic (Chapter 4) - 4 lectures
5. Synchronous Sequential Logic (Chapter 5) - 4 lectures
6. Registers and Counters (Chapter 6) - 4 lectures
7. Memory and Programmable Logic (Chapter 7) - 3 lectures

No classes: March 15 and 17 (Spring Break)
March 31 (Cesar Chavez Birthday)

Key Dates: TBD (Mid-term exam)
May 12 (Last day of classes)
May 19: 2:00 – 3:50 pm (Final exam)