

# CES 522: VLSI Design

## Course Outline Fall '09

### Instructor:

Dr. Mohammad Rafiqul Haider, Ph. D. Email: [haider@sonoma.edu](mailto:haider@sonoma.edu)

**Days:** Wednesday

**Times:** 6:00 pm to 8:50 pm

**Location:** Salazar Hall 2003

**Office Hours:** Monday (4:00 – 5:00), Tuesday and Thursday (2:30 – 3:30), Wednesday (5:00 - 6:00)

**Office:** 2010B Salazar Hall

**Phone:** (707)-664-3462

**Pre-Requisite:** CES 530 or by instructor's approval

**Course Description:** This class covers basic understandings of very large scale integration (VLSI) ranging from MOS level design to subsystem design. The course will cover the following sections:

- Basic concepts of VLSI, historical background, circuit and system representation in VLSI, Hardware description language (HDL), Verilog
- MOS theory, nonlinear effects, DC characteristics of CMOS inverter
- Performance estimation, resistance and capacitance characteristics, distributed RC effects, calculation of rise time, fall time, delay time, calculation of power dissipation
- CMOS circuit and logic design, NAND, NOR, CMOS, pseudo-nMOS, Dynamic CMOS, clocked CMOS, pass transistors, clocking strategies
- Analog CMOS subsystem design, two stage opamp design
- Digital CMOS subsystem design, adder, subtractor, parity generators, binary counters, ALU, memory elements

### Course Material:

Principles of CMOS VLSI Design: A system perspective, 2<sup>nd</sup> edition

Neil H. E. Weste and Kamran Eshraghian

Addison Wesley

### Reference Books:

[1] R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*, 3<sup>rd</sup> Ed., McGraw Hill.

[2] Grey, Hurst, Lewis and Meyer, *Analysis and Design of Analog Integrated Circuits*, 4<sup>th</sup> Ed. Wiley.

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill

[4] R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, Prentice Hall.

[5] B. Razavi, *RF Microelectronics*, Prentice Hall.

[6] Franco Maloberti, *Analog Design for CMOS VLSI Systems*, Kluwer Academic Press

[7] S.M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits* (3<sup>rd</sup> Edition), McGraw Hill Companies

<b>Examinations</b>	<b>Percentage</b>
Midterm @ 100 points	<b>20%</b>
Final @ 100 points	<b>30%</b>
2 Projects @ 100 points	<b>40%</b>
Attendance	<b>10%</b>
<b>Total</b>	<b>100%</b>

<b>Grading Scale</b>	
90-100%	<b>A</b>
80-89%	<b>B</b>
70-79%	<b>C</b>
60-69%	<b>D</b>
0-59%	<b>F</b>

**Class Policy:**

All teaching guidelines and policies of SSU apply to this class. In order to get credit for an exam the student must notify the instructor prior to a class session if they will be unable to attend (and reschedule for a different date).

**Attendance:**

Attendance is mandatory. There will be no excused absences except in the case of emergencies that could be substantiated.

**Examinations:**

Each student is expected to keep up with the assignments. Examinations are based upon theory and practice material and may include multiple choice, true/false, short answers, and problems. Exams and projects marks will be scaled to take into account the overall class performance.

**Projects:**

Two projects will be assigned during the semester. The project topic will be chosen by the instructor in collaboration with the student.

**Policy on the Submission of Project Work:**

1. All projects must be done individually unless instructed otherwise.
2. Tables and graphs in the project submissions must be neat and clean with proper explanation.
4. Each project submission is due in the beginning of the class on the specified date.

Failing to do any of the above, a submission may not be accepted resulting in the loss of grade in that assignment.

**Success:**

To be successful in this class we suggest the following:

- Attend all classes (or communicate to the instructor)
- Listen attentively
- Take notes
- Participate in discussions
- Attempt all homework
- Form study groups

**Class Schedule:**

<b>Class</b>	<b>Topic</b>	<b>Material Covered</b>
1	VLSI Concept and Hardware description language (HDL)	Basic understanding of VLSI, system representation, system architecture, design procedures, Introduction to Verilog®
2	MOS transistor theory	nMOS and pMOS enhancement transistors, MOS device equations, nonlinearities
3	MOS transistor theory	CMOS inverter, DC characteristics, Architectures of different types of inverters, transmission gate, BiCMOS inverter
4	CMOS circuit design and logic design	CMOS logic gate design, transistor sizing, complex logic gate design, CMOS logic, pseudo-nMOS logic, Dynamic CMOS logic, clocked CMOS logic, pass transistor logic
5	CMOS circuit design and logic design	Clocking strategies, clocked systems, latches and registers, two phase clocking, four phase clocking
6	Circuit characterization and performance estimation	Calculation of resistance and capacitance, MOS-capacitor characteristics, distributed RC effects, switching characteristics, Rise time, Fall time and delay time
7	10/14/2009	<b>Mid Term Examination</b>
8	Circuit characterization and performance estimation	CMOS gate transistor sizing, cascaded complementary inverters, stage ratio, power dissipation, static, dynamic and total power dissipation, superbuffer
9	CMOS processing technology	Basic n-well and p-well process, metal interconnect, polysilicon, resistors, capacitors, design rules
10	CMOS processing technology	Design rules, layer representations, stick diagram, latchup, origin of latchup and prevention mechanisms
11	Analog CMOS subsystem design	Analog layout, matching, opamp design
12	CMOS subsystem design	Different implementations of Adder and Subtractors

13	CMOS subsystem design	Parity generators, comparators, zero/one detector, binary counter, Multiplication
14	CMOS subsystem design	Memory elements
15		<b>Review</b>
16	12/16/2009	<b>Final Examination</b>

**Outcomes:**

By attending this course students will learn

1. an ability to apply knowledge of mathematics, science, and engineering
2. an ability to design a system, component, or process to meet desired needs within realistic constraints
3. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

**Academic Honesty:**

You are responsible to behave ethically & honestly. Copying, cheating, forgery, and other unethical or dishonest actions are not tolerated.

See [http://www.sonoma.edu/uaffairs/policies/cheating\\_plagiarism.htm](http://www.sonoma.edu/uaffairs/policies/cheating_plagiarism.htm)

**Important Dates:**

- September 9, last day to add
- September 22, Last day to Drop with 'W' (done online)
- November 7, Last day to Petition to Withdraw from a Class