

CMOS VLSI Design

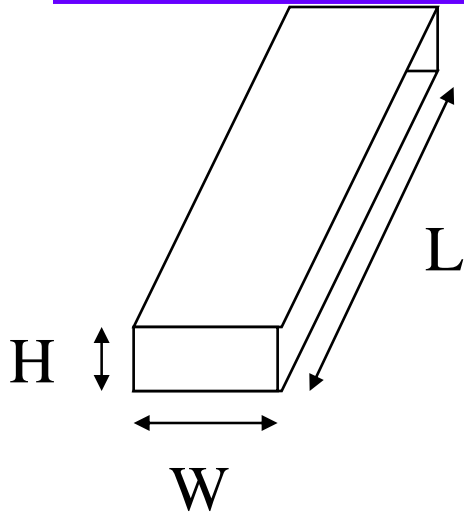
Lecture 03

Sonoma State University

Outline

- Wire Resistance
- Inverter Circuit
- Different types of Inverters
- CMOS Inverter
- DC Response

Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho L}{HW}$$

Sheet Resistance R_{\square}

$$R_{1\square} = R_{2\square}$$

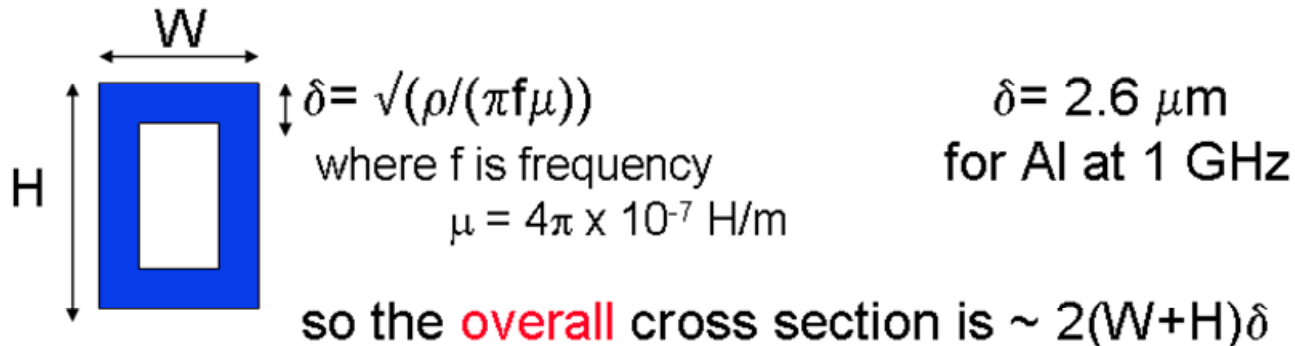


| Material | $\rho(\Omega\text{-m})$ |
|---------------|-------------------------|
| Silver (Ag) | 1.6×10^{-8} |
| Copper (Cu) | 1.7×10^{-8} |
| Gold (Au) | 2.2×10^{-8} |
| Aluminum (Al) | 2.7×10^{-8} |
| Tungsten (W) | 5.5×10^{-8} |

| Material | Sheet Res. (Ω/\square) |
|--------------------------------|---------------------------------|
| n, p well diffusion | 1000 to 1500 |
| n+, p+ diffusion | 50 to 150 |
| n+, p+ diffusion with silicide | 3 to 5 |
| polysilicon | 150 to 200 |
| polysilicon with silicide | 4 to 5 |
| Aluminum | 0.05 to 0.1 |

Skin Effect

- At high frequency, currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially with depth into the wire

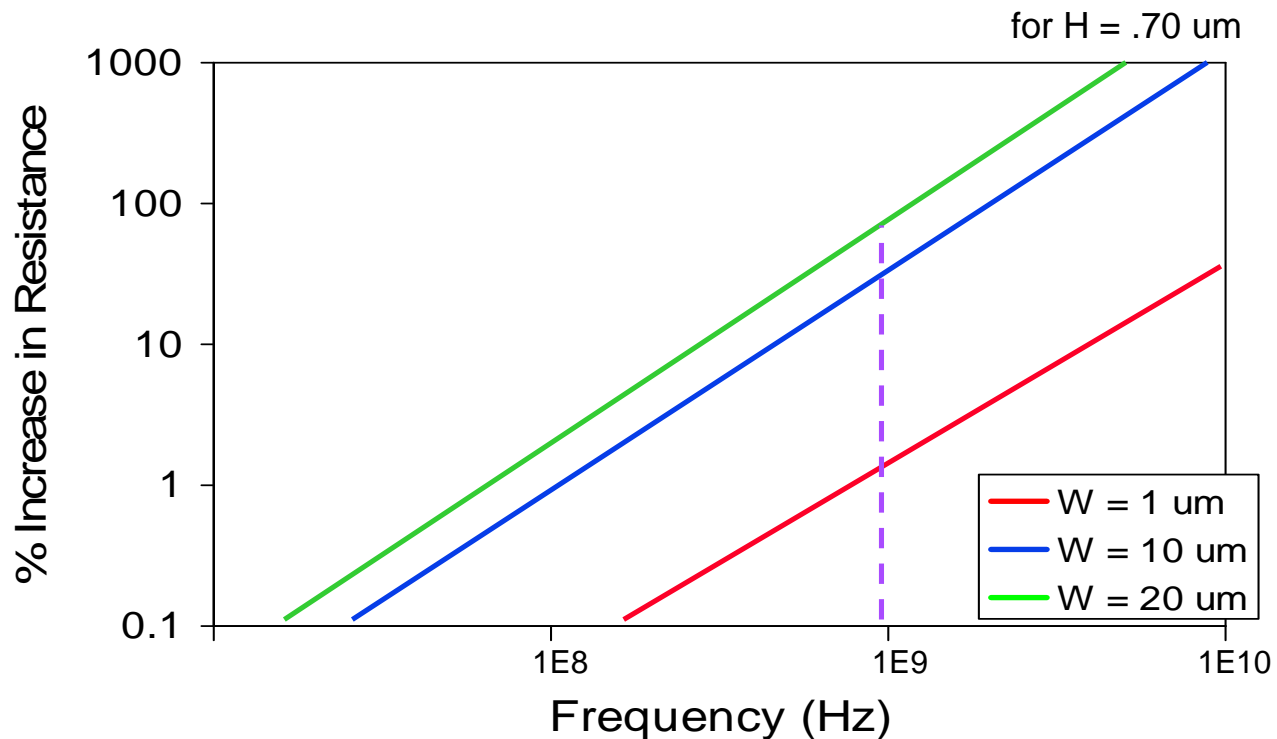


- The onset of skin effect is at f_s - where the skin depth is equal to half the largest dimension of the wire.

$$f_s = 4 \rho / (\pi \mu (\max(W, H))^2)$$

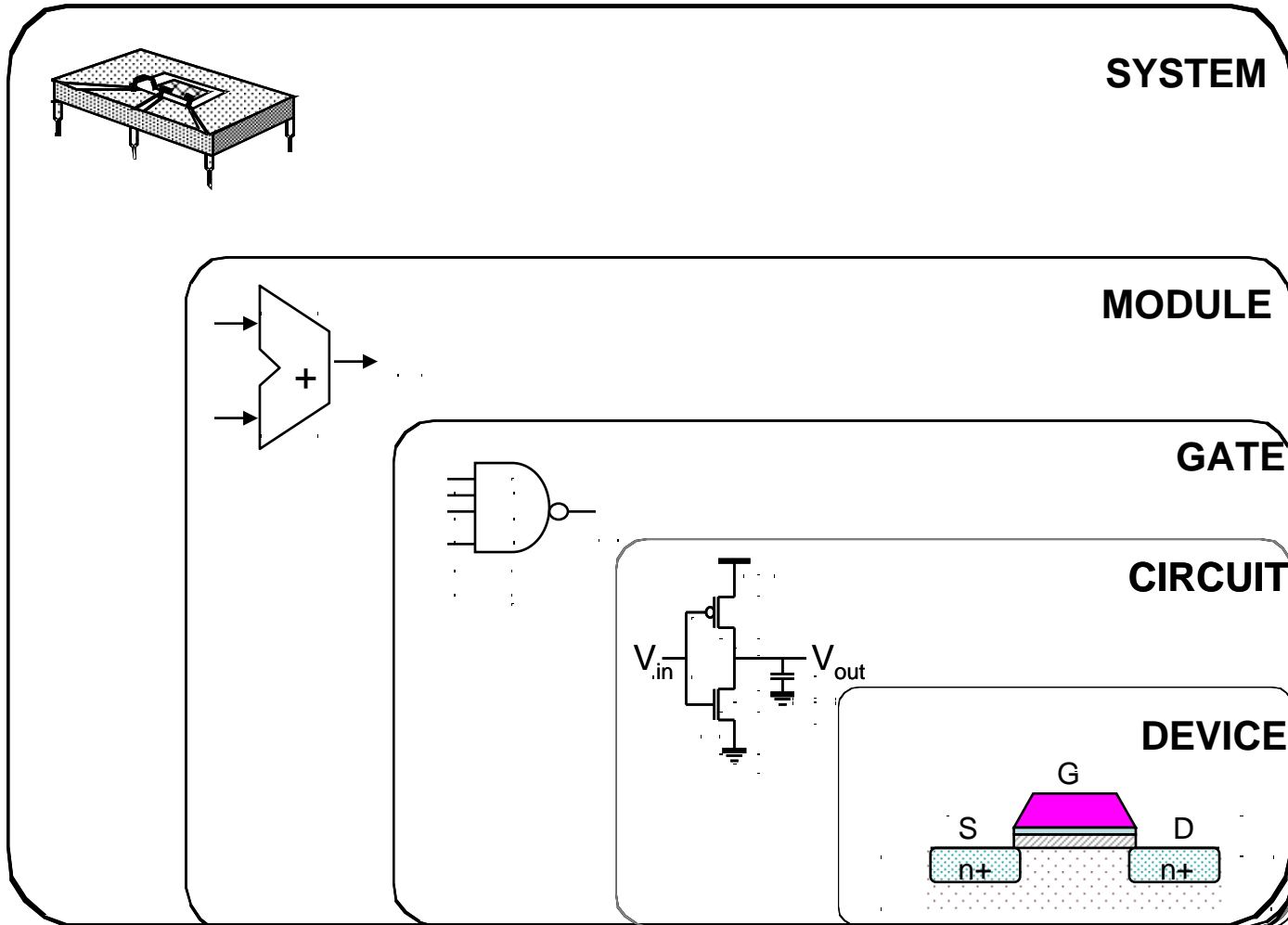
- An issue for high frequency, wide (tall) wires (i.e., clocks!)

Skin Effect for Different W



- A 30% increase in resistance is observed for 20 μm Al wires at 1 GHz (versus only a 1% increase for 1 μm wires)

Design Abstract Level



Activity

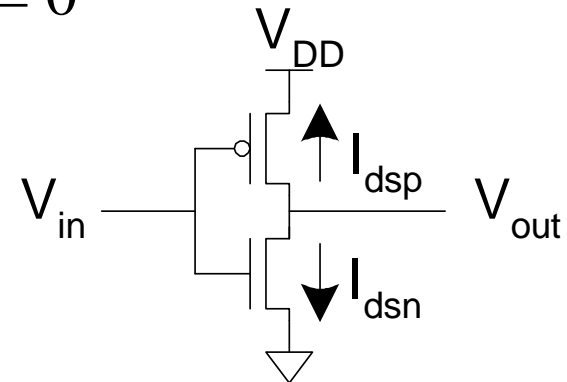
- 1) If the width of a transistor increases, the current will
increase decrease not change
- 2) If the length of a transistor increases, the current will
increase decrease not change
- 3) If the supply voltage of a chip increases, the maximum transistor current will
increase decrease not change
- 4) If the width of a transistor increases, its gate capacitance will
increase decrease not change
- 5) If the length of a transistor increases, its gate capacitance will
increase decrease not change
- 6) If the supply voltage of a chip increases, the gate capacitance of each transistor will
increase decrease not change

Activity

- 1) If the width of a transistor increases, the current will
increase decrease not change
- 2) If the length of a transistor increases, the current will
increase **decrease** not change
- 3) If the supply voltage of a chip increases, the maximum transistor current will
increase decrease not change
- 4) If the width of a transistor increases, its gate capacitance will
increase decrease not change
- 5) If the length of a transistor increases, its gate capacitance will
increase decrease not change
- 6) If the supply voltage of a chip increases, the gate capacitance of each transistor will
increase decrease **not change**

DC Response

- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
 - When $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
 - When $V_{in} = V_{DD} \rightarrow V_{out} = 0$
 - In between, V_{out} depends on transistor size and current
 - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
 - We could solve equations
 - But graphical solution gives more insight

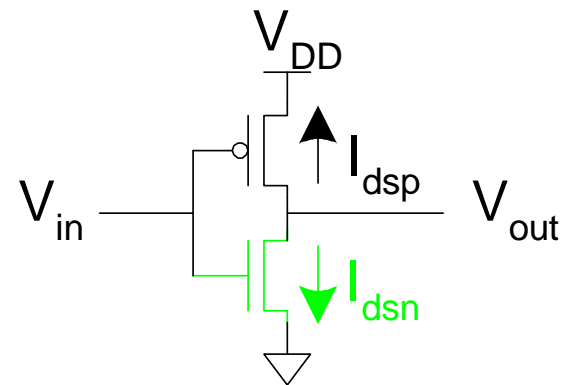


Transistor Operation

- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
 - Cutoff?
 - Linear?
 - Saturation?

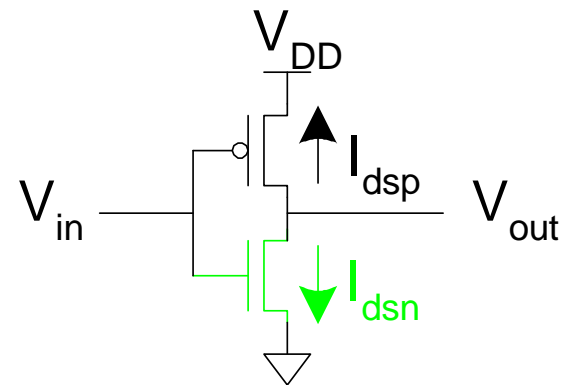
nMOS Operation

| Cutoff | Linear | Saturated |
|-------------|-------------|-------------|
| $V_{gsn} <$ | $V_{gsn} >$ | $V_{gsn} >$ |
| | $V_{dsn} <$ | $V_{dsn} >$ |



nMOS Operation

| Cutoff | Linear | Saturated |
|--------------------|------------------------------|------------------------------|
| $V_{gsn} < V_{tn}$ | $V_{gsn} > V_{tn}$ | $V_{gsn} > V_{tn}$ |
| | $V_{dsn} < V_{gsn} - V_{tn}$ | $V_{dsn} > V_{gsn} - V_{tn}$ |

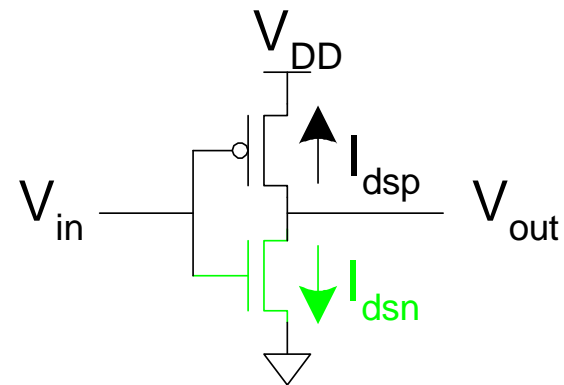


nMOS Operation

| Cutoff | Linear | Saturated |
|--------------------|------------------------------|------------------------------|
| $V_{gsn} < V_{tn}$ | $V_{gsn} > V_{tn}$ | $V_{gsn} > V_{tn}$ |
| | $V_{dsn} < V_{gsn} - V_{tn}$ | $V_{dsn} > V_{gsn} - V_{tn}$ |

$$V_{gsn} = V_{in}$$

$$V_{dsn} = V_{out}$$

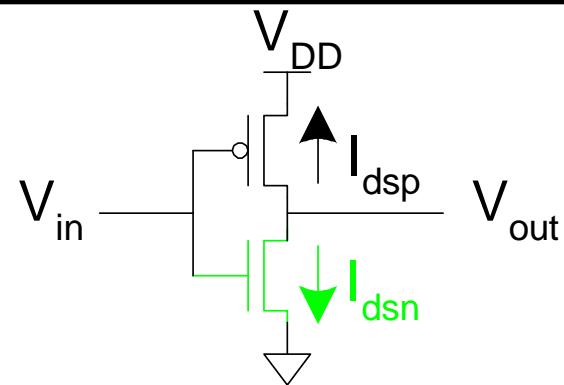


nMOS Operation

| Cutoff | Linear | Saturated |
|---|--|--|
| $V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$ | $V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$ | $V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$ |

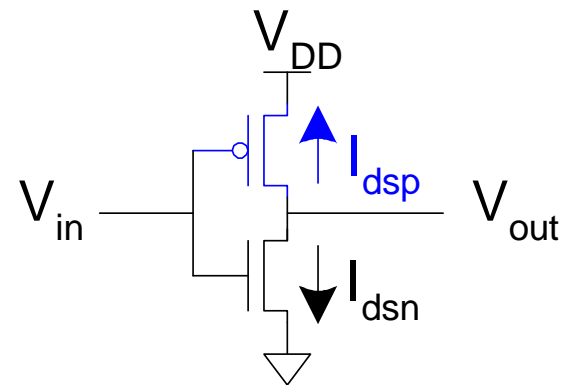
$$V_{gsn} = V_{in}$$

$$V_{dsn} = V_{out}$$



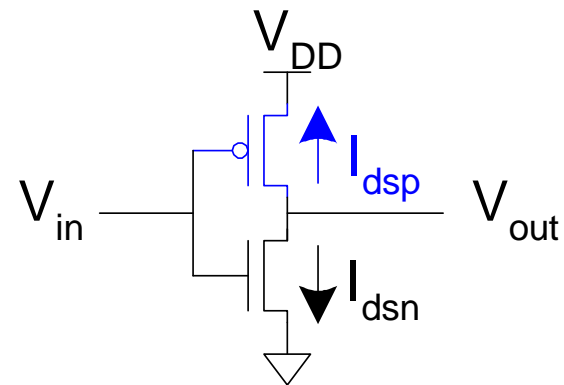
pMOS Operation

| Cutoff | Linear | Saturated |
|-------------|-------------|-------------|
| $V_{gsp} >$ | $V_{gsp} <$ | $V_{gsp} <$ |
| | $V_{dsp} >$ | $V_{dsp} <$ |



pMOS Operation

| Cutoff | Linear | Saturated |
|--------------------|------------------------------|------------------------------|
| $V_{gsp} > V_{tp}$ | $V_{gsp} < V_{tp}$ | $V_{gsp} < V_{tp}$ |
| | $V_{dsp} > V_{gsp} - V_{tp}$ | $V_{dsp} < V_{gsp} - V_{tp}$ |



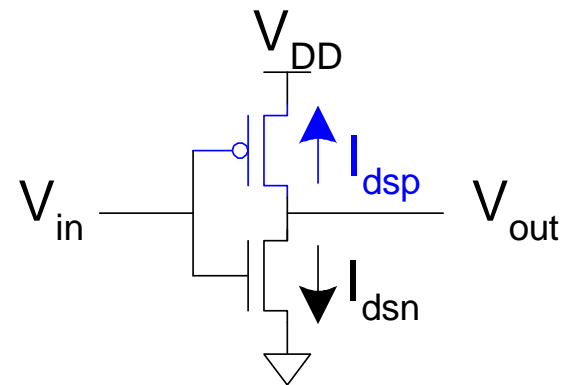
pMOS Operation

| Cutoff | Linear | Saturated |
|--------------------|------------------------------|------------------------------|
| $V_{gsp} > V_{tp}$ | $V_{gsp} < V_{tp}$ | $V_{gsp} < V_{tp}$ |
| | $V_{dsp} > V_{gsp} - V_{tp}$ | $V_{dsp} < V_{gsp} - V_{tp}$ |

$$V_{gsp} = V_{in} - V_{DD}$$

$$V_{tp} < 0$$

$$V_{dsp} = V_{out} - V_{DD}$$



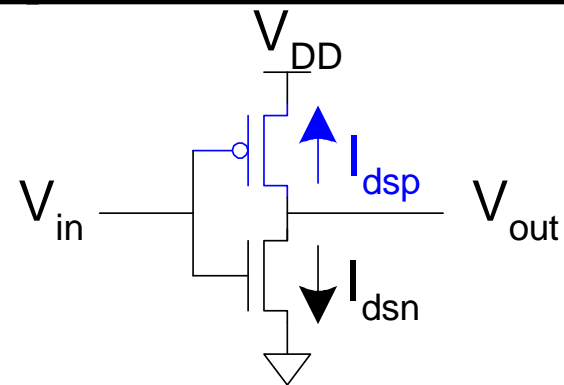
pMOS Operation

| Cutoff | Linear | Saturated |
|--|---|---|
| $V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$ | $V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{DD} - V_{tp}$ | $V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{DD} - V_{tp}$ |

$$V_{gsp} = V_{in} - V_{DD}$$

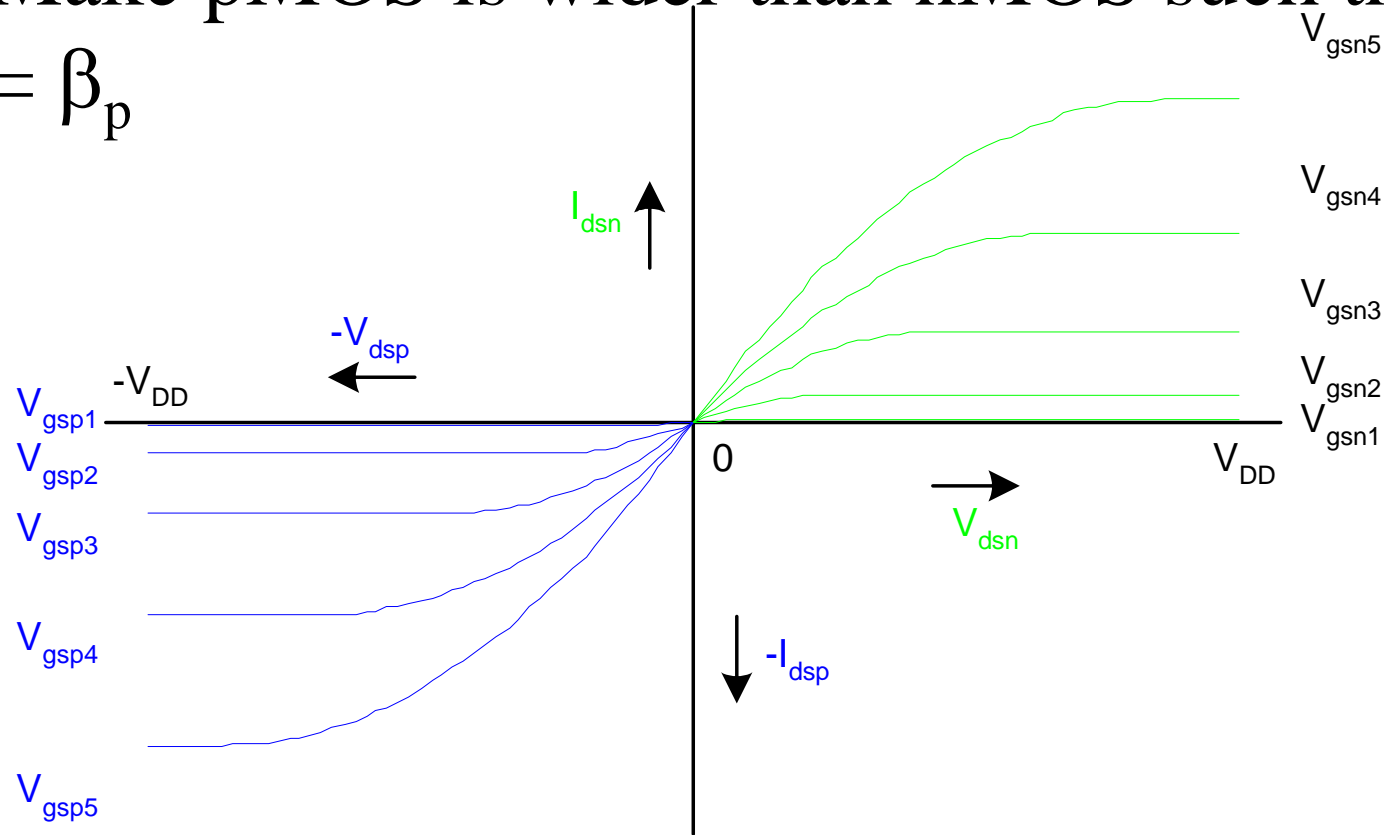
$$V_{tp} < 0$$

$$V_{dsp} = V_{out} - V_{DD}$$

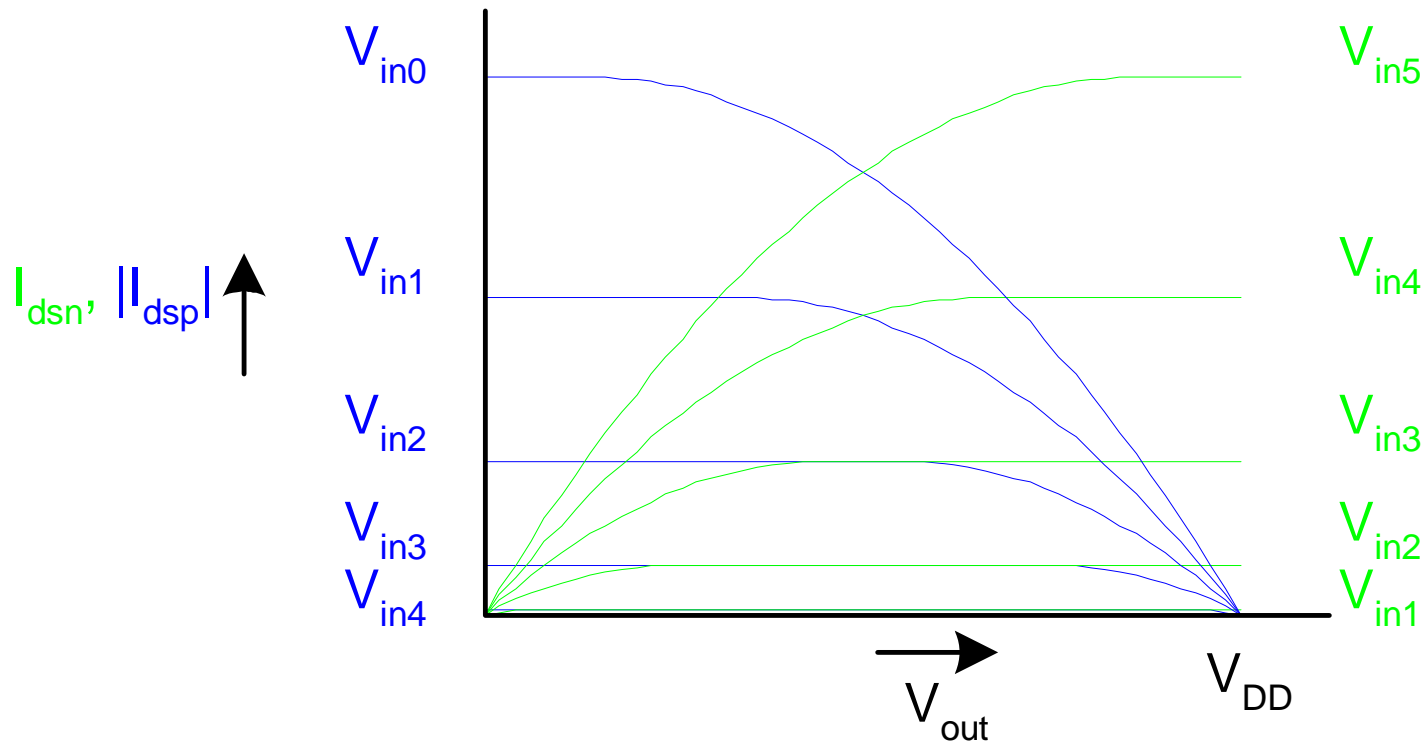


I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

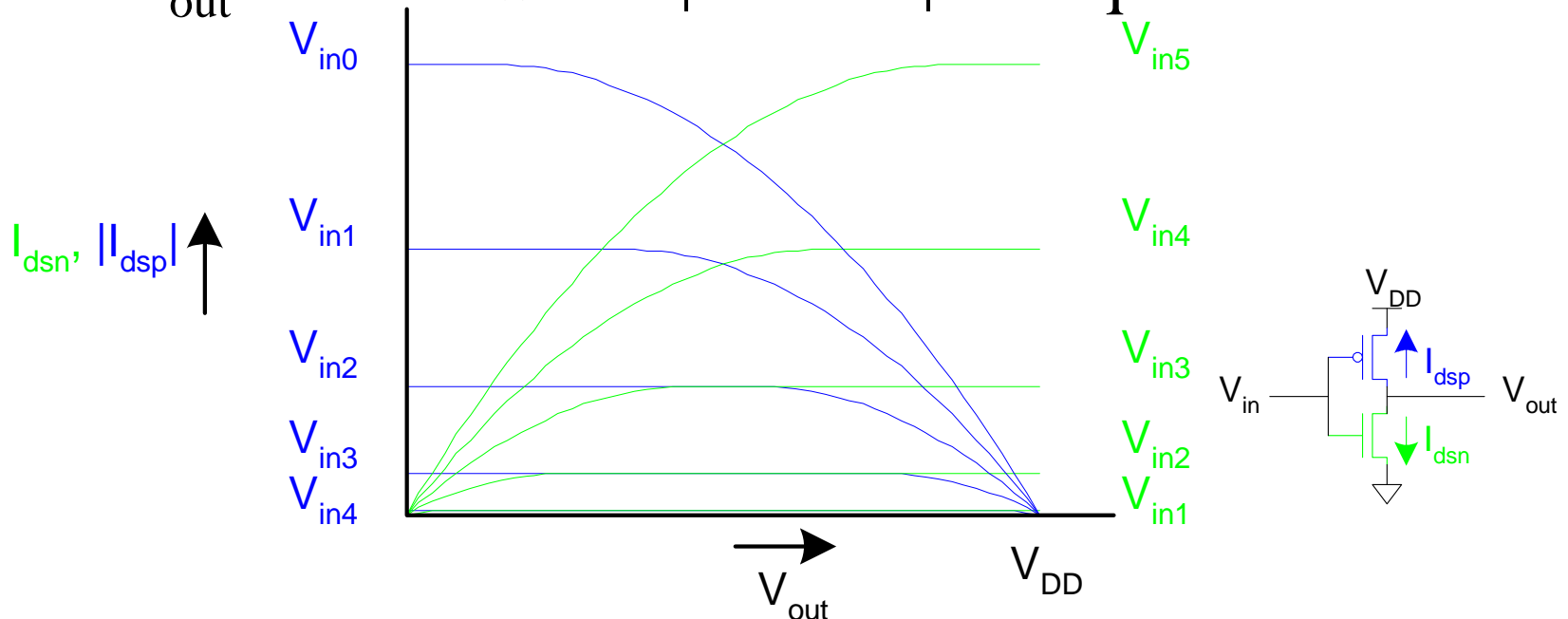


Current vs. V_{out} , V_{in}



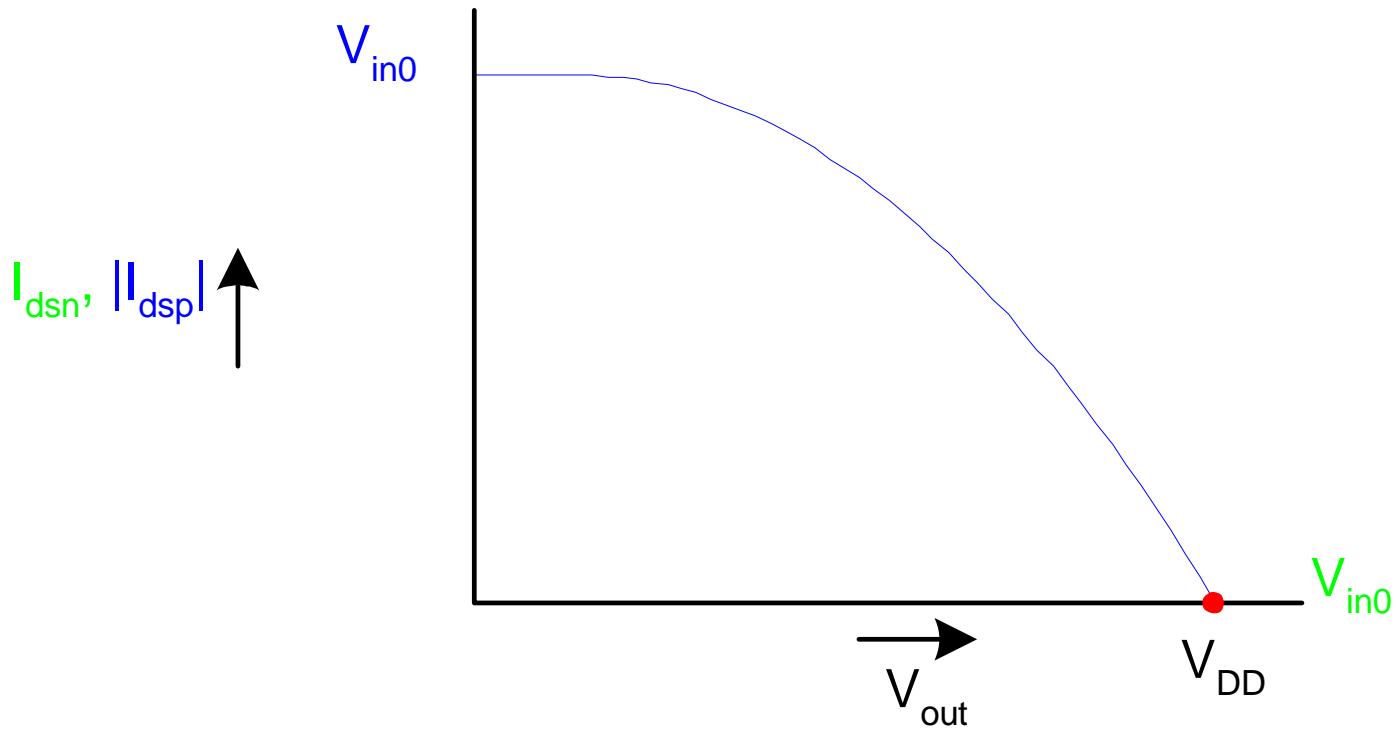
Load Line Analysis

- For a given V_{in} :
 - Plot I_{dsn} , I_{dsp} vs. V_{out}
 - V_{out} must be where |currents| are equal in



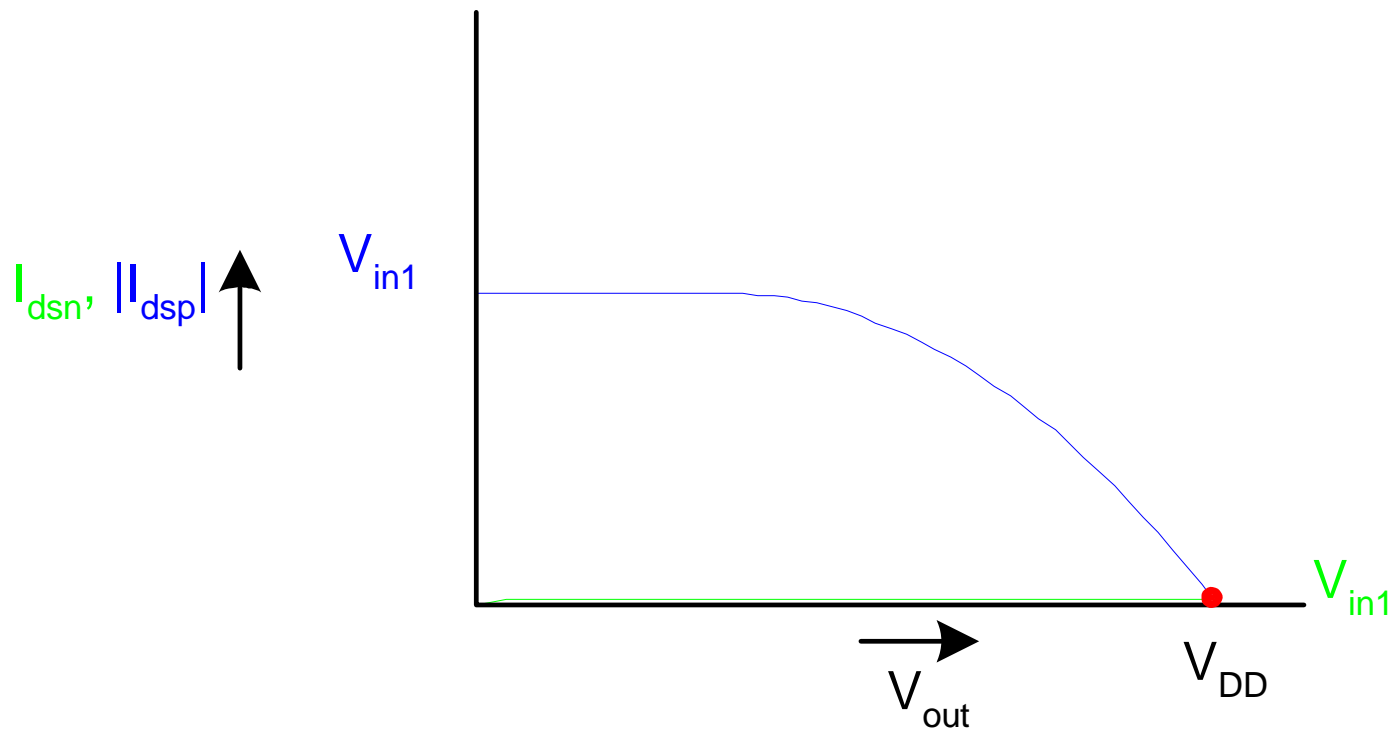
Load Line Analysis

- $V_{in} = 0$



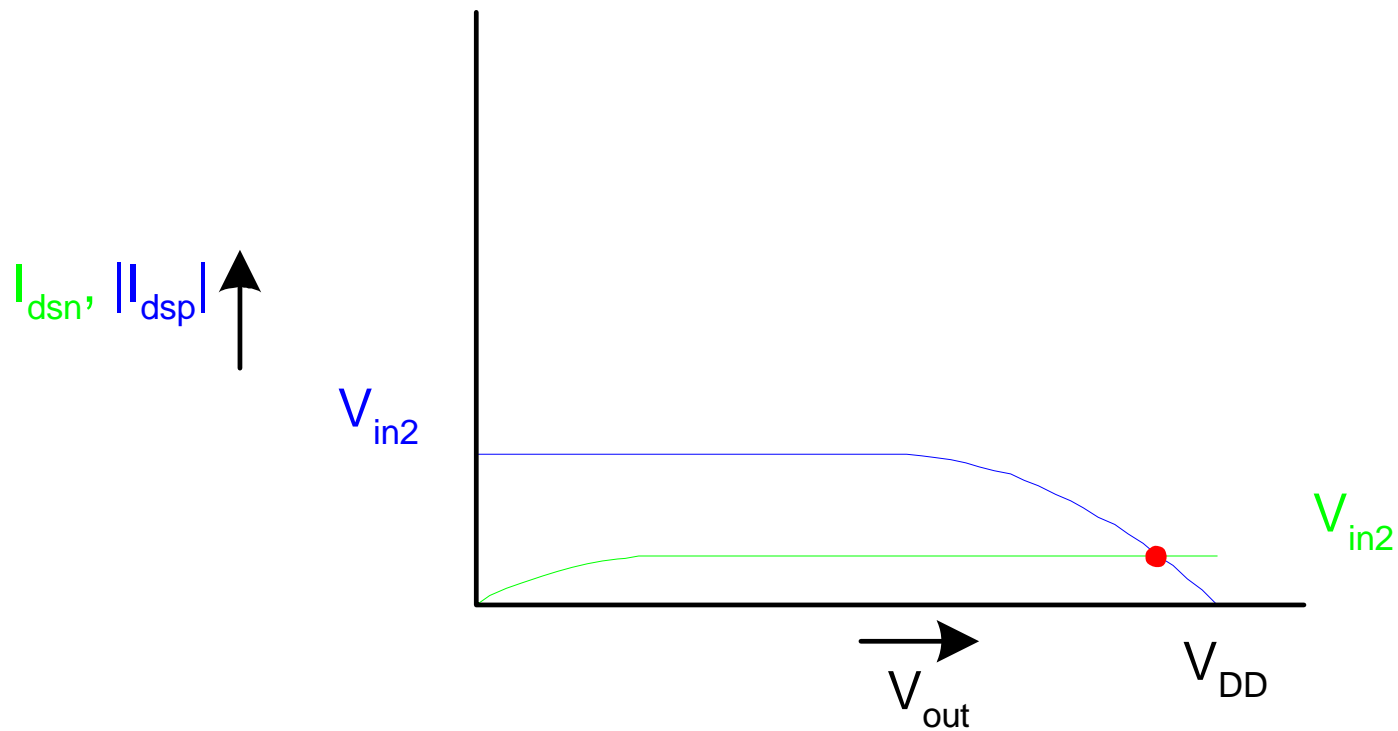
Load Line Analysis

- $V_{in} = 0.2V_{DD}$



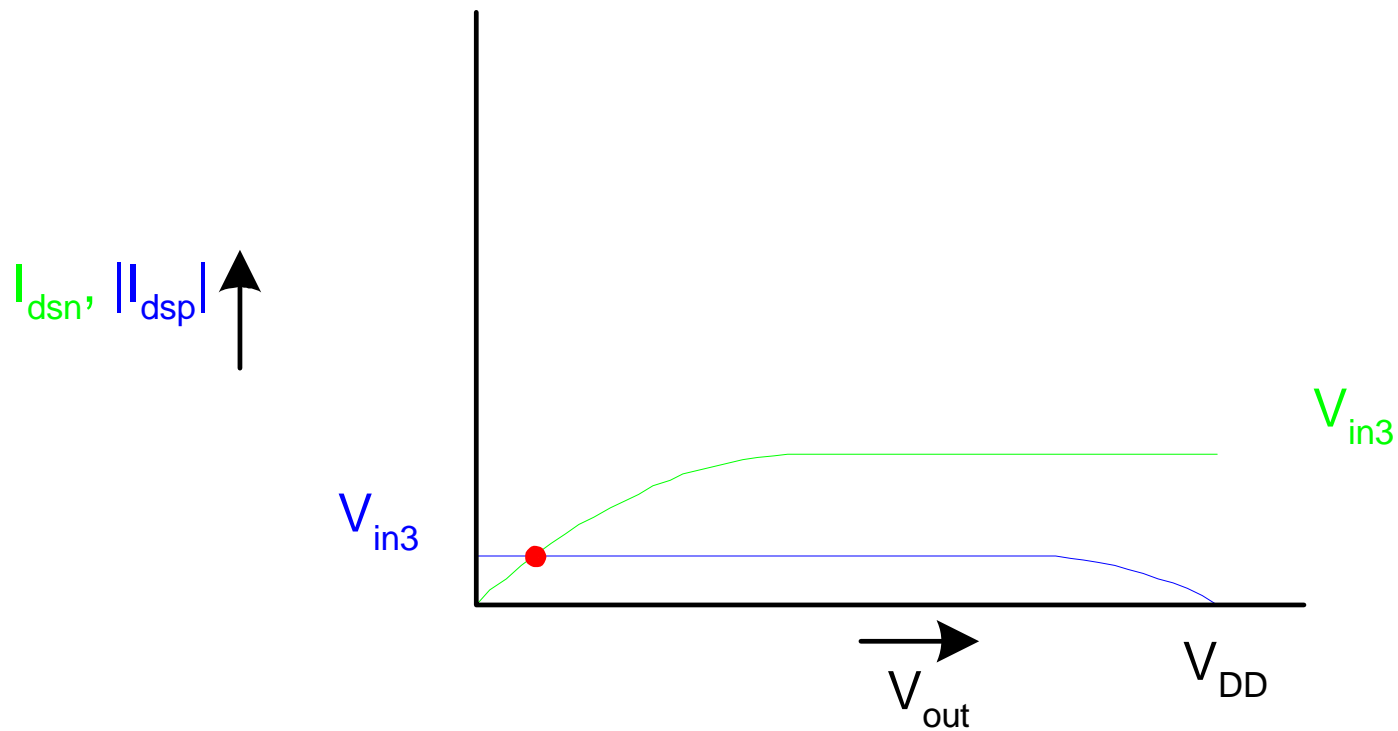
Load Line Analysis

- $V_{in} = 0.4V_{DD}$



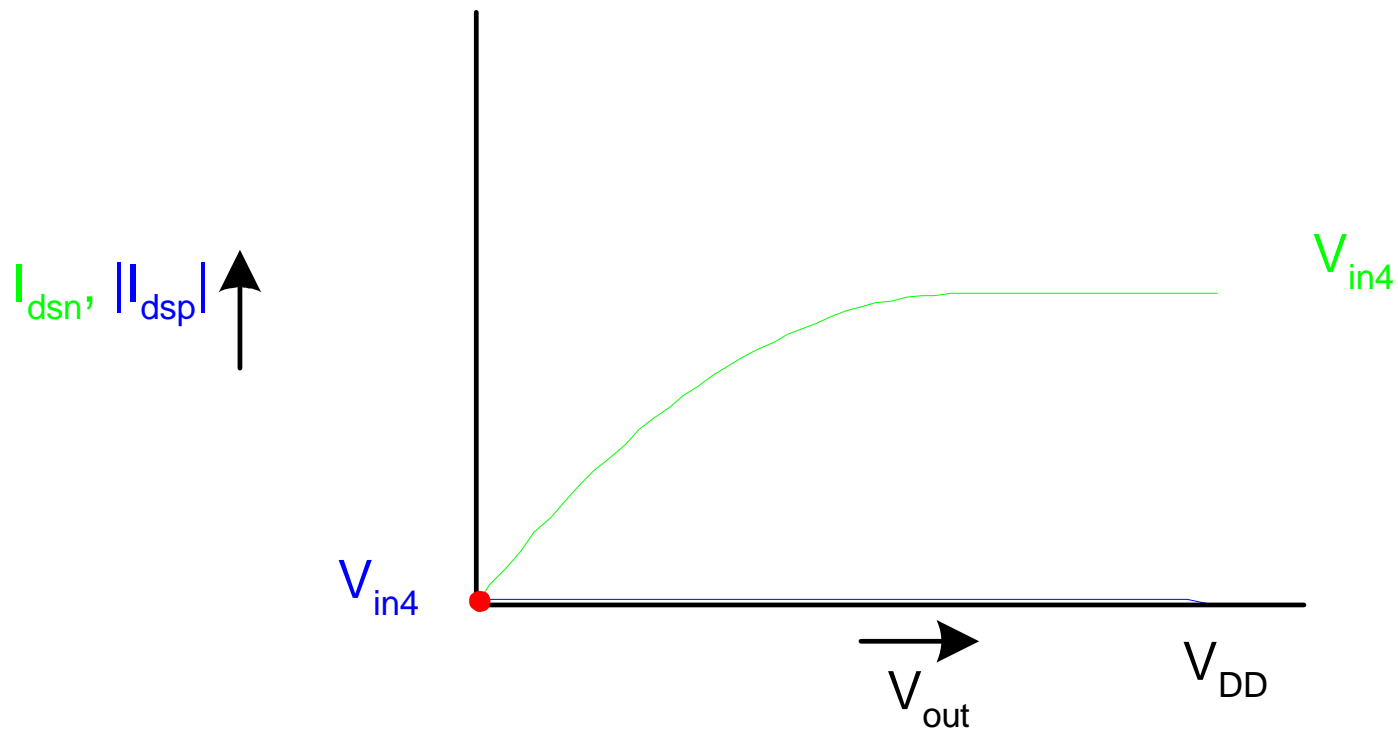
Load Line Analysis

- $V_{in} = 0.6V_{DD}$



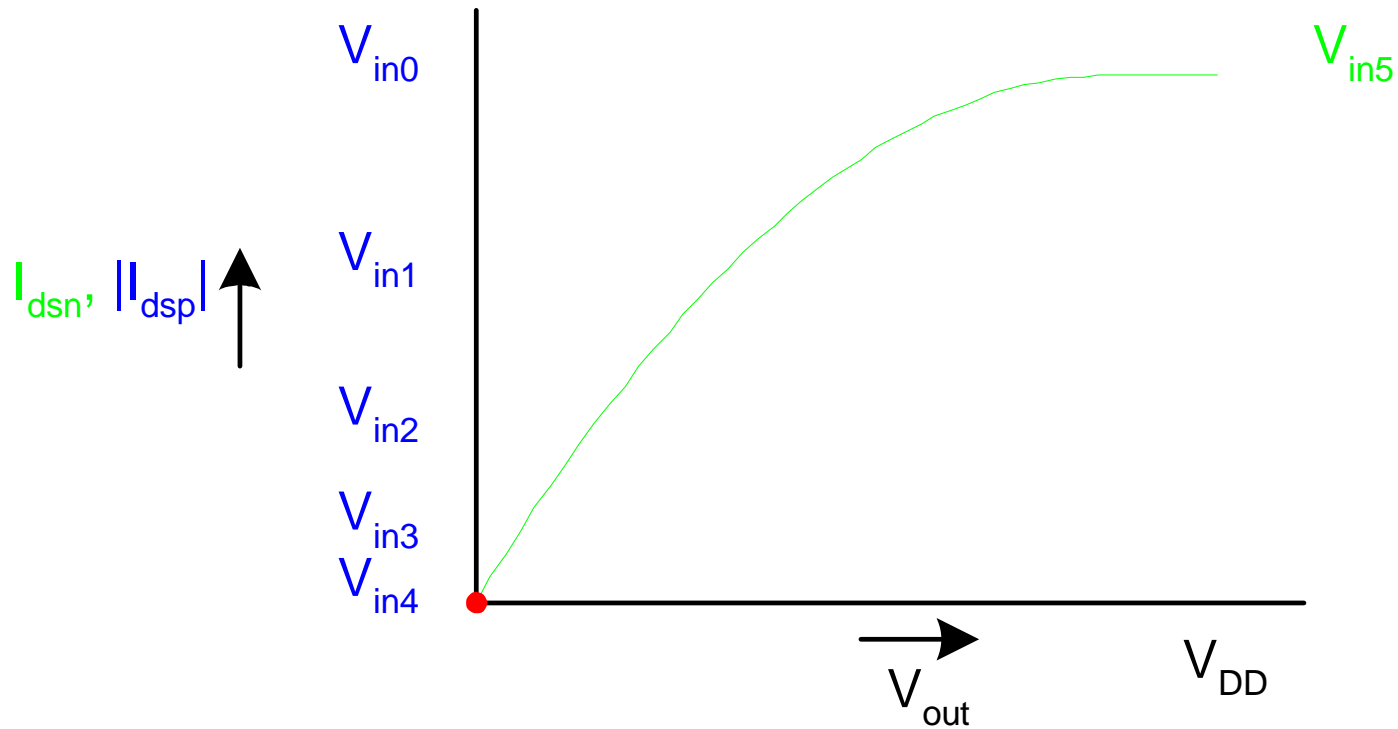
Load Line Analysis

- $V_{in} = 0.8V_{DD}$

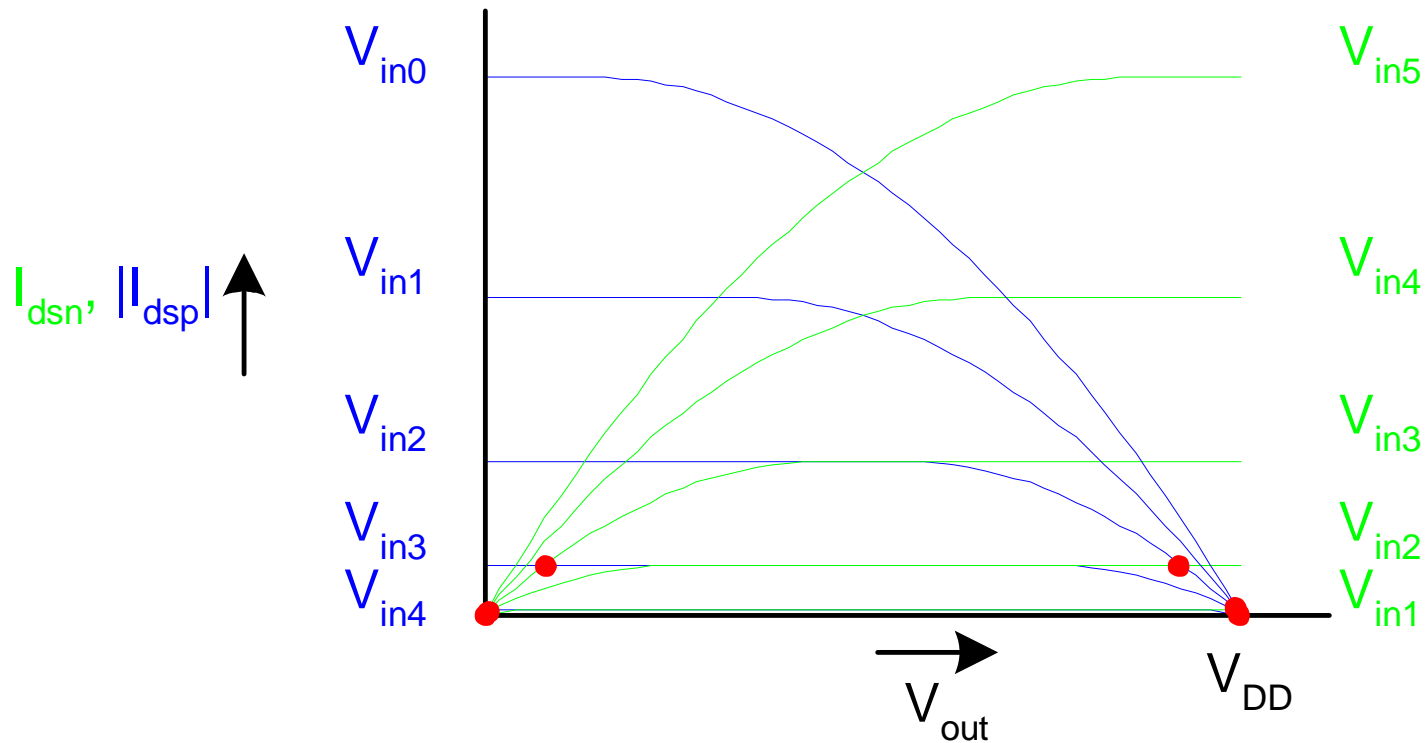


Load Line Analysis

- $V_{in} = V_{DD}$

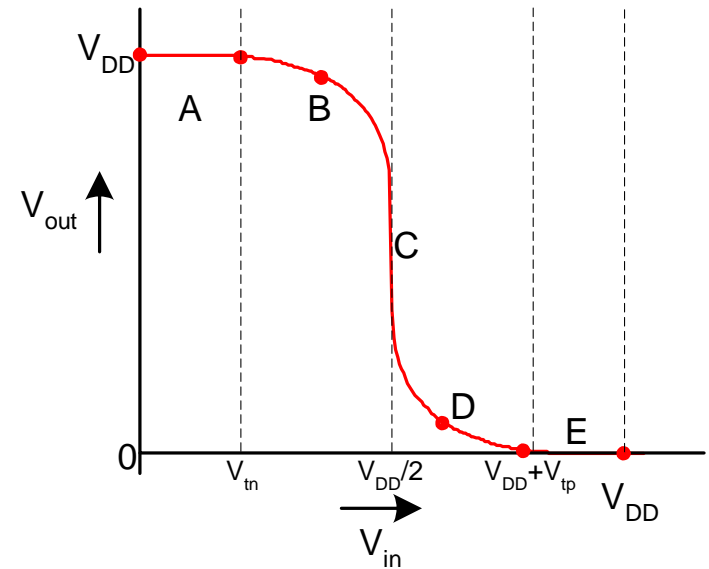
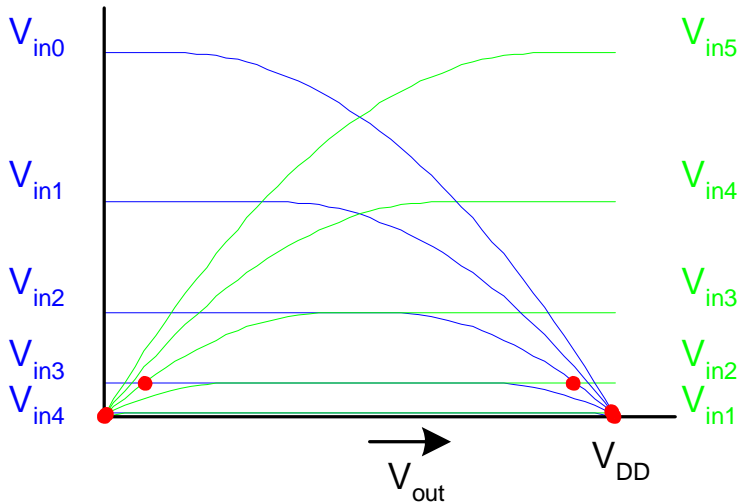


Load Line Summary



DC Transfer Curve

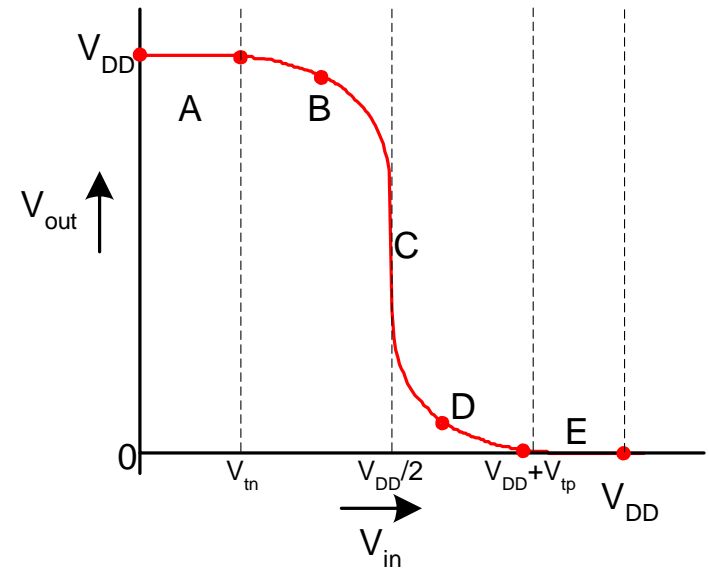
- Transcribe points onto V_{in} vs. V_{out} plot



Operating Regions

- Revisit transistor operating regions

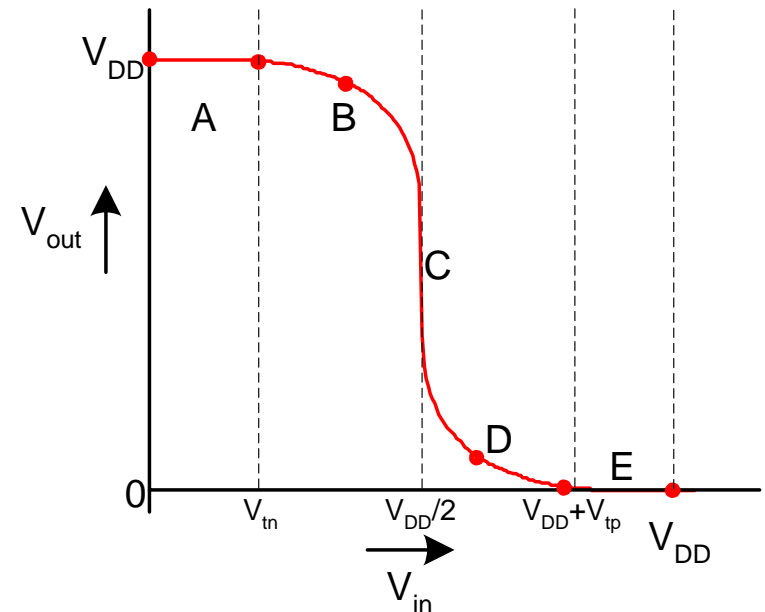
| Region | nMOS | pMOS |
|--------|------|------|
| A | | |
| B | | |
| C | | |
| D | | |
| E | | |



Operating Regions

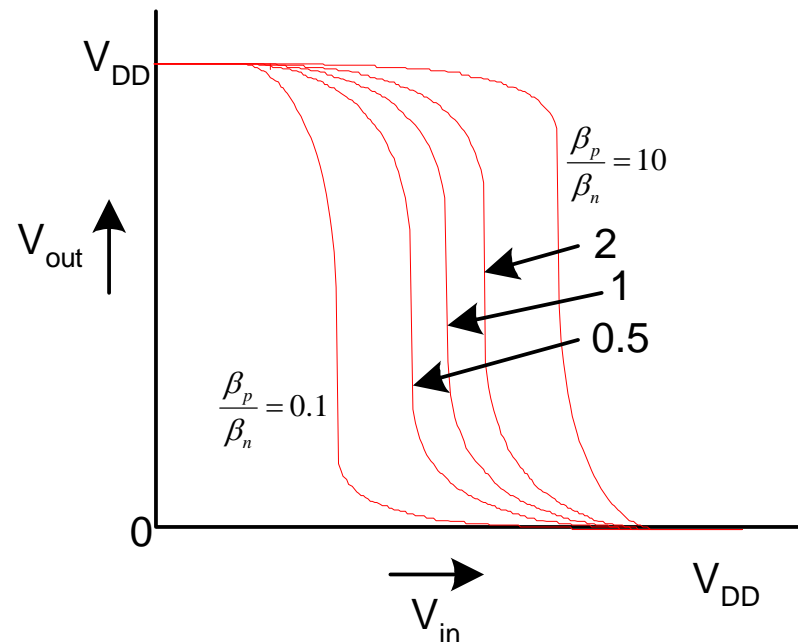
- Revisit transistor operating regions

| Region | nMOS | pMOS |
|--------|------------|------------|
| A | Cutoff | Linear |
| B | Saturation | Linear |
| C | Saturation | Saturation |
| D | Linear | Saturation |
| E | Linear | Cutoff |



Beta Ratio

- If $b_p / b_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



W/L Calculation

$$I_{ds} = K \frac{W}{L} \left\{ (V_{gs} - V_t) V_{ds} - \frac{1}{2} V_{ds}^2 \right\} \quad \text{For Linear Region of Operation}$$

$$I_{ds} = K \frac{W}{2L} (V_{gs} - V_t)^2$$

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2 \quad \text{For Saturation Region of Operation}$$

W/L Calculation

Both PMOS and NMOS are working in the saturation region

$$I_{dsn} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2 \quad \text{For NMOS}$$

$$I_{sdp} = \frac{\beta_p}{2} (V_{sg} - |V_{tp}|)^2$$
$$= \frac{\beta_p}{2} (V_{DD} - V_{in} - |V_{tp}|)^2 \quad \text{For PMOS}$$

Now Equate $I_{dsn} = I_{sdp}$

W/L Calculation

$$I_{dsn} = I_{sdp}$$

$$\Rightarrow \frac{\beta_n}{2} (V_{in} - V_{tn})^2 = \frac{\beta_p}{2} (V_{DD} - V_{in} - |V_{tp}|)^2$$

$$\Rightarrow \sqrt{\frac{\beta_n}{\beta_p}} = \frac{V_{DD} - V_{in} - |V_{tp}|}{V_{in} - V_{tn}}$$

$$\Rightarrow \sqrt{\frac{\beta_n}{\beta_p}} (V_{in} - V_{tn}) = V_{DD} - V_{in} - |V_{tp}|$$

$$\Rightarrow V_{in} \left(1 + \sqrt{\frac{\beta_n}{\beta_p}} \right) = V_{DD} - |V_{tp}| + V_{tn} \sqrt{\frac{\beta_n}{\beta_p}}$$

$$\therefore V_{in} = \frac{V_{DD} - |V_{tp}| + V_{tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = V_{out} = V_{TH}$$

If $V_{tn} = |V_{tp}|$ and $\beta_n = \beta_p$

$$V_{in} = V_{DD}/2$$

For $\beta_n = \beta_p$,

$$\mu_p W_p/L_p = \mu_n W_n/L_n$$

$$W_p/L_p = 2.5 W_n/L_n$$

Series and Parallel MOS Connection

- Series –

$$R_{eq} = R_1 + R_2$$

$$\Rightarrow 1/(W/L)_{eq} = 1/(W/L)_1 + 1/(W/L)_2$$

$$\Rightarrow (L/W)_{eq} = (L/W)_1 + (L/W)_2$$

$$\Rightarrow (L/W)_{eq} = 2(L/W)$$

$$\Rightarrow \mathbf{L/W = L/(2*W)}$$

- Parallel –

$$R_{eq} = 1/R_1 + 1/R_2$$

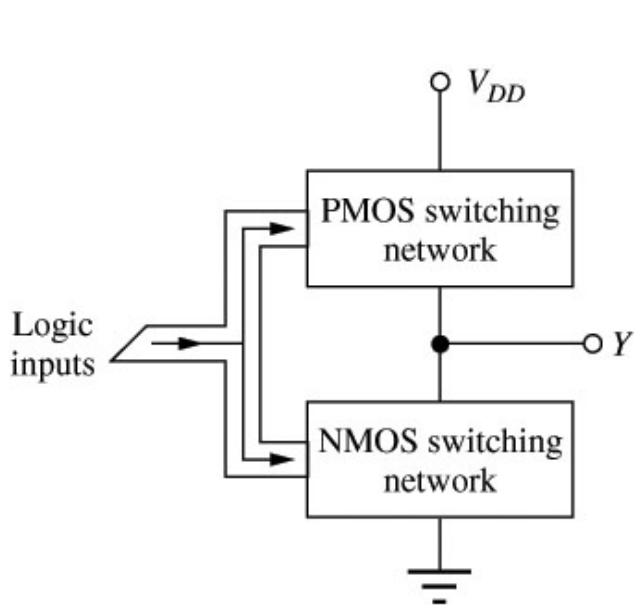
$$\Rightarrow (W/L)_{eq} = (W/L)_1 + (W/L)_2$$

$$\Rightarrow (W/L)_{eq} = 2(W/L) \Rightarrow \mathbf{W/L = 0.5*(W/L)_{eq}}$$

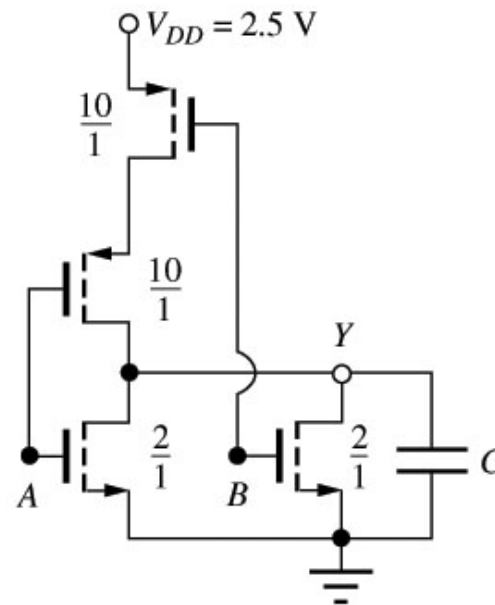
Worst Case Design

- Design is always focused on an equivalent inverter design
- Worst case
 - All the series MOS are on
 - Only one of the parallel MOS is on

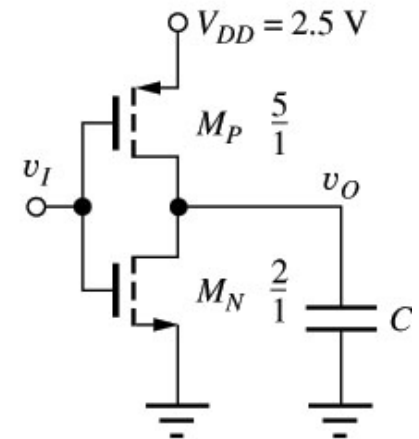
CMOS NOR Gate



Basic CMOS logic gate structure

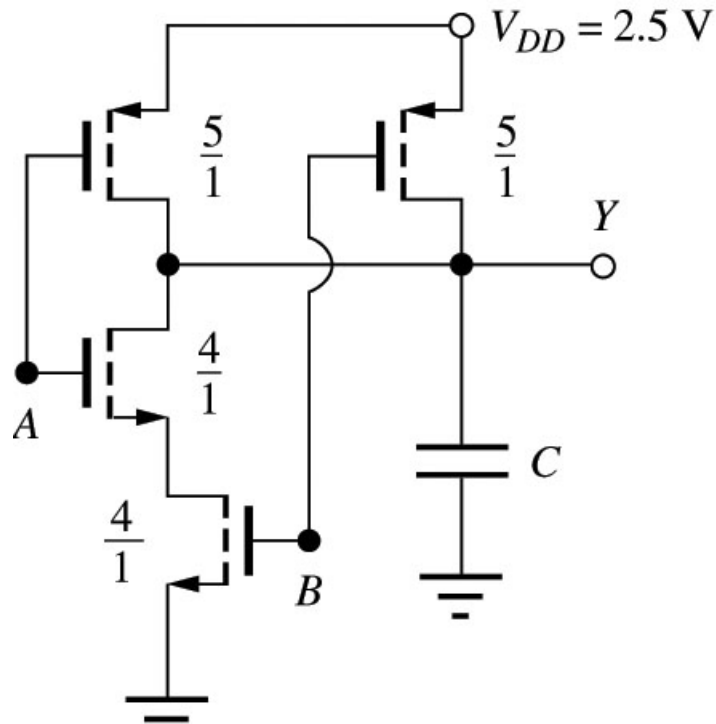


CMOS NOR gate implementation

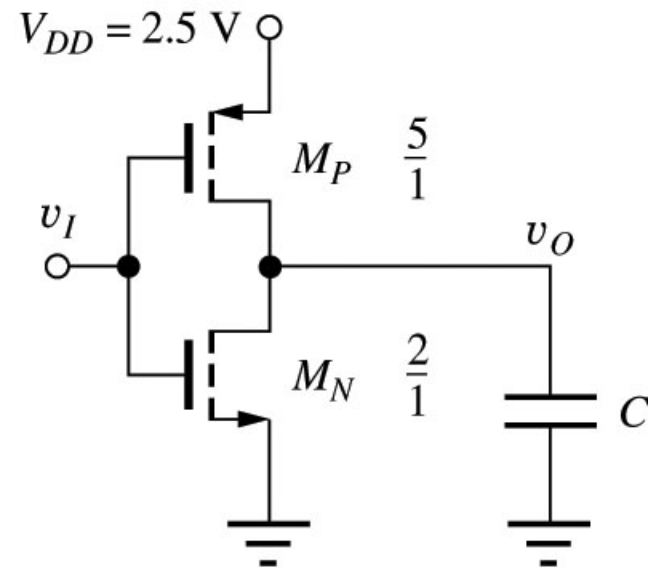


Reference Inverter

CMOS NAND Gates



CMOS NAND gate
implementation

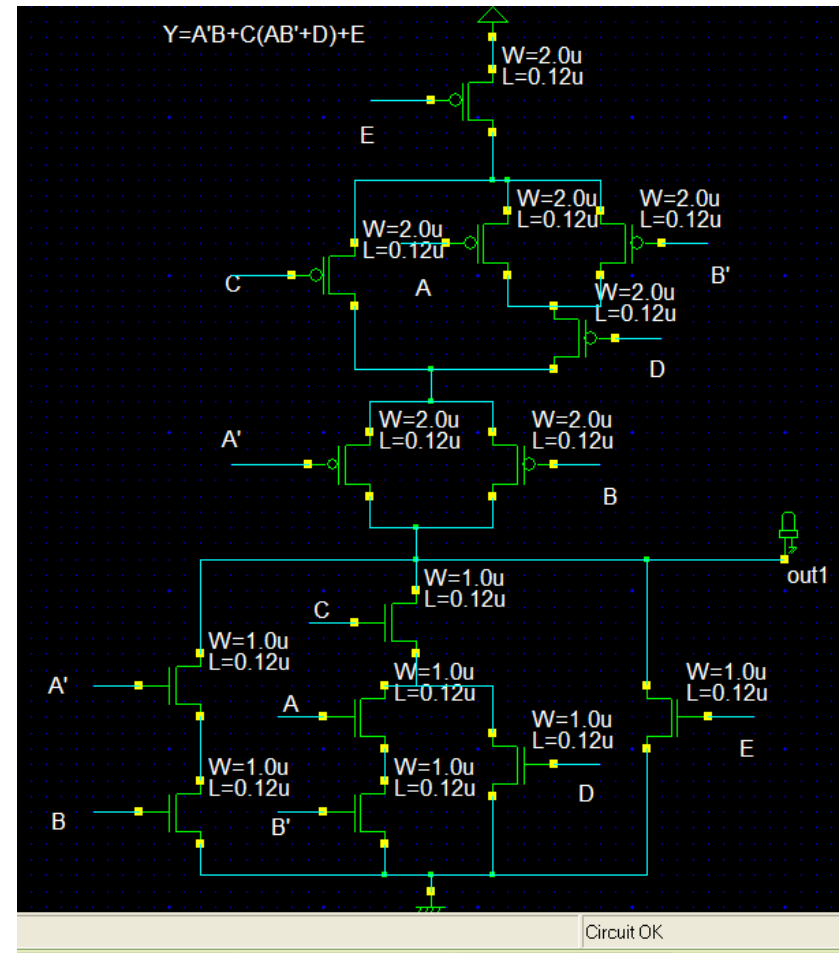
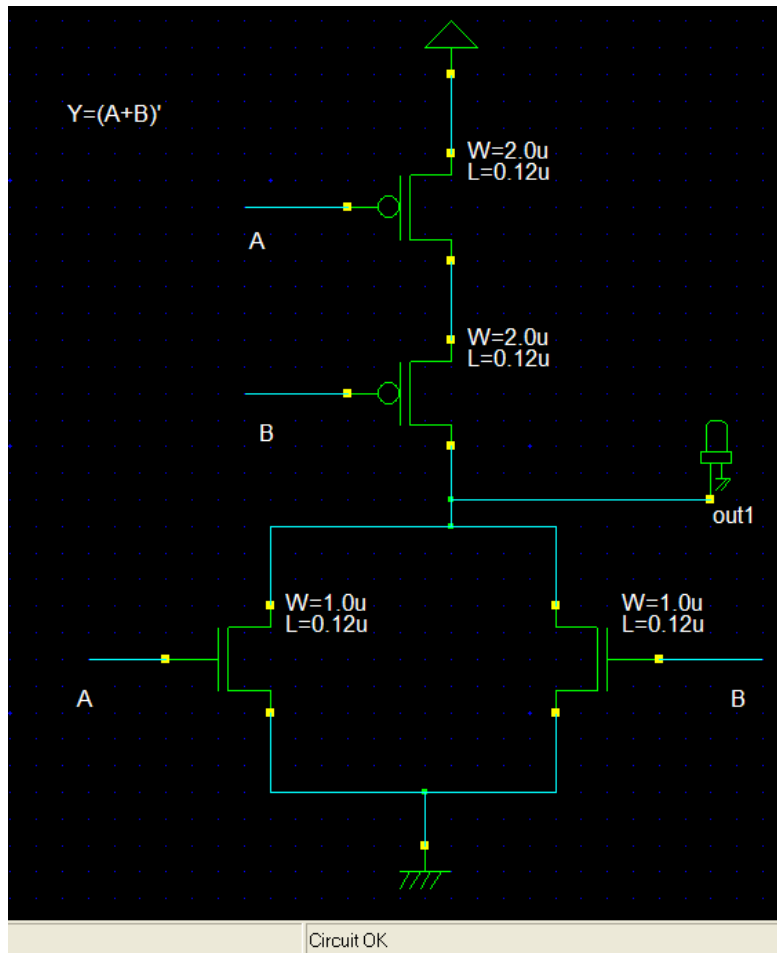


Reference Inverter

Arbitrary Logic Implementation

- Standard logic circuit – AND, NAND, OR etc.
- Circuit for arbitrary logic – $Y=A'B+B'C$
- Assume all types of inputs are available
- + means parallel combination
- . means series combination
- Use MOSFET sizing ratio
- Output is inverted
- Use additional inverter to generate correct output
- Generate all the input signals.

CMOS Circuit Design



Transistor Sizing

Equivalent inverter design. Equal pull-up and pull-down current.

MOSFET in series connection

$$\frac{1}{(W/L)_{eq}} = \frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \dots \dots + \frac{1}{(W/L)_N}$$

MOSFET in parallel connection

$$(W/L)_{eq} = (W/L)_1 + (W/L)_2 + \dots \dots + (W/L)_N$$

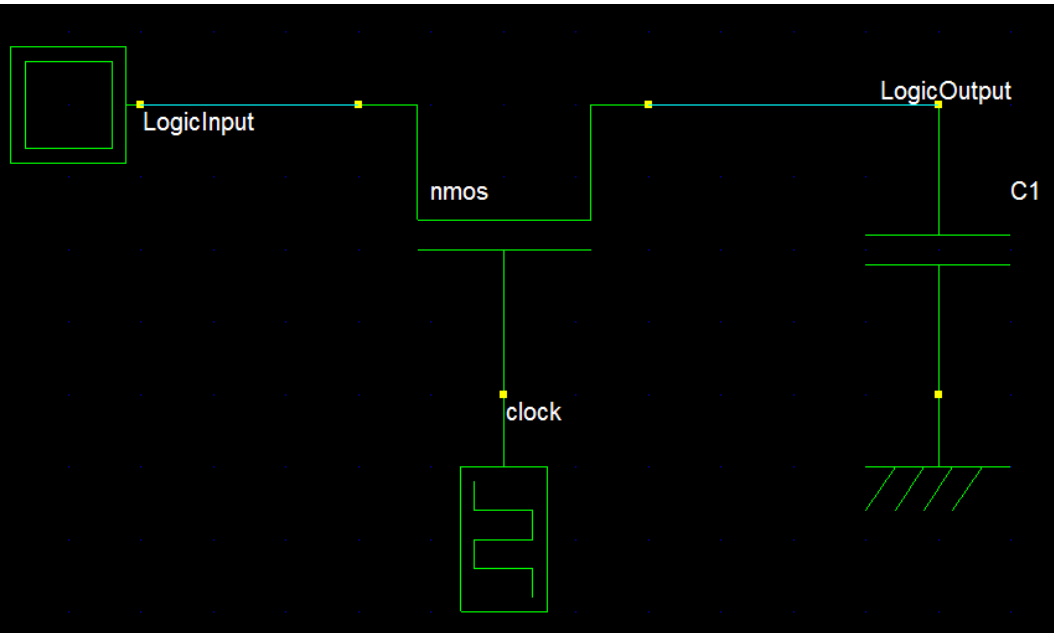
Transistor Sizing

- Worst case analysis.
- 3 NMOS in series. $W/L=3n=4 \times 1.5=6=3.0/0.5$
- 2 NMOS in series $W/L=2n=3=1.5/0.5$
- 4 PMOS in series $W/L=4p=4 \times 2 \times 1.5=12=6/0.5$
- 3 PMOS in series

$$\frac{1}{p} = \frac{1}{4p} + \frac{1}{4p} + \frac{1}{(W/L)_2}$$

$$(W/L)_2 = 2p = 2 \times 1.5 \times 2 = 6 = 3/0.5$$

Pass Transistor Logic



Clock=0, No change

Clock = 1, four different cases could arise

Case (1): $V_{in}=V_{out}=0$, no current flow, no change.

Case (2): $V_{in}=V_{out}=1$, no current flow, no change.

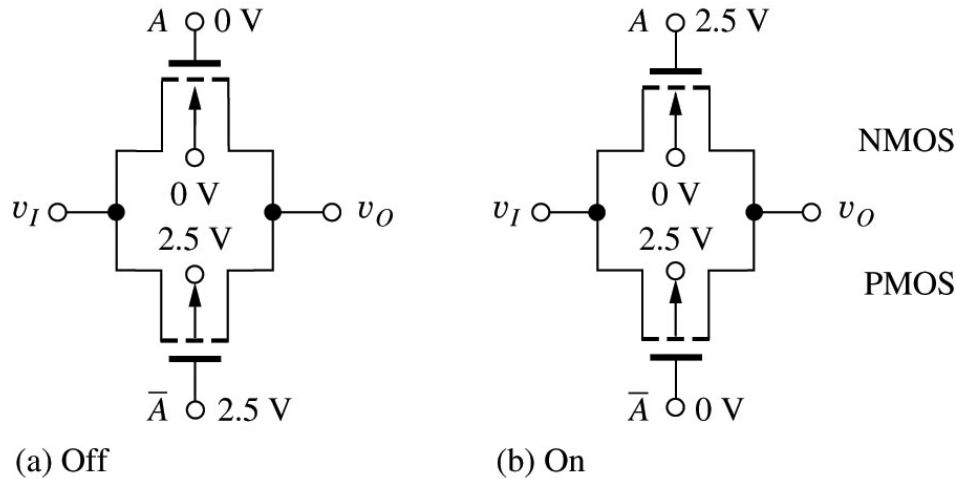
Case (3): $V_{in}=1, V_{out}=0$, current flows, V_{out} becomes $(V_{in}-V_t)$

Case (4): $V_{in}=0, V_{out}=1$, current flows, V_{out} becomes 0.

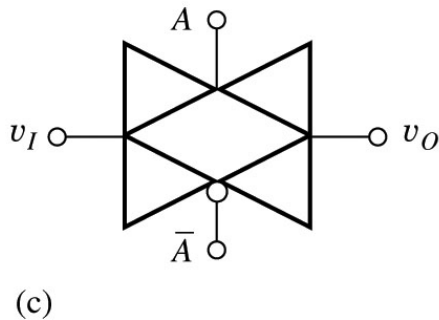
NMOS pass transistor is good for logic 0 transfer but not for logic 1 transfer.

Creates weak logic 1.

Transmission Gate



- The CMOS transmission gate (T-gate) is a useful circuits for both analog and digital applications



- It acts as a switch that can operate up to V_{DD} and down to V_{SS}

Other Inverters

- Resistive Load Inverter
- NMOS Enhancement Load Inverter
- NMOS Depletion Load Inverter