
Switching Characteristics and Delay

Review: CMOS inverter: V_{TH}

□ KCL:

$$\frac{k_n}{2} (V_{GS,n} - V_{T0,n})^2 = \frac{k_p}{2} (V_{GS,p} - V_{T0,p})^2$$

$$\frac{k_n}{2} (V_{in} - V_{T0,n})^2 = \frac{k_p}{2} (V_{in} - V_{CC} - V_{T0,p})^2$$

□ Solve for $V_{TH} = V_{in} = V_{out}$

$$V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} (V_{CC} + V_{T0,p})}{1 + \sqrt{\frac{1}{k_R}}}$$

$$k_R = \frac{k_n}{k_p}$$

CMOS inverter: Ideal V_{TH} (Symmetrical, $K_n=K_p$)

$$V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} (V_{CC} + V_{T0,p})}{1 + \sqrt{\frac{1}{k_R}}}$$

$$k_R = \frac{k_n}{k_p}$$

□ Ideally, $V_{th} = V_{CC}/2$

□ Assuming $V_{T0,n} = V_{T0,p}$,

$$k_{R,ideal} = \left(\frac{V_{CC}/2 + V_{T0,p}}{V_{CC}/2 + V_{T0,n}} \right)^2$$

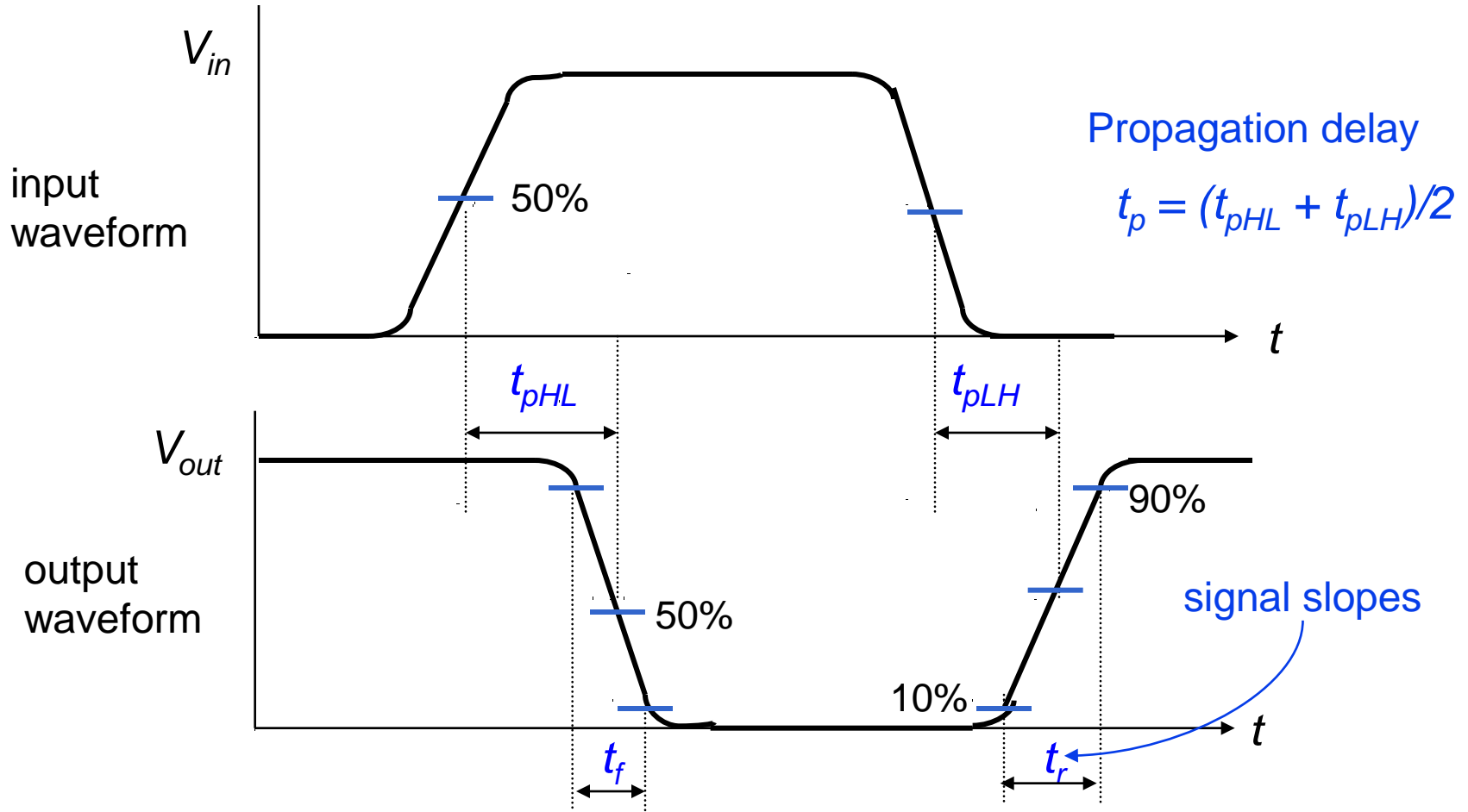
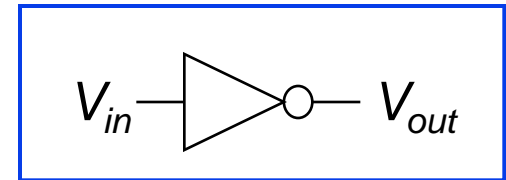
$$k_{R,ideal} = 1$$

For ideal symmetrical inverter required that

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p} \approx 2.5 \quad \Rightarrow \quad \left(\frac{W}{L}\right)_n \approx 2.5 \left(\frac{W}{L}\right)_p$$

Delay Definitions

The propagation delay t_p of a gate defines how quickly it responds to a change at its input(s).



Inverter delay

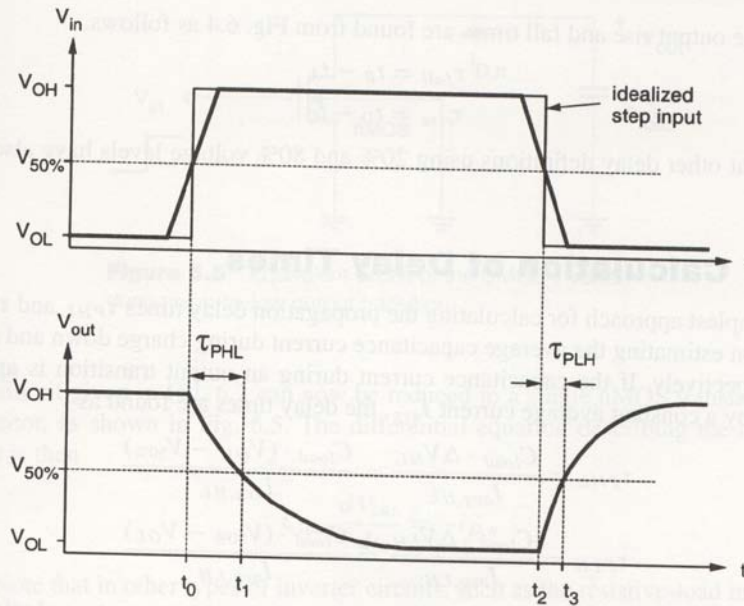


Figure 6.3 Input and output voltage waveforms of a typical inverter, and the definitions of propagation delay times. The input voltage waveform is idealized as a step pulse for simplicity.

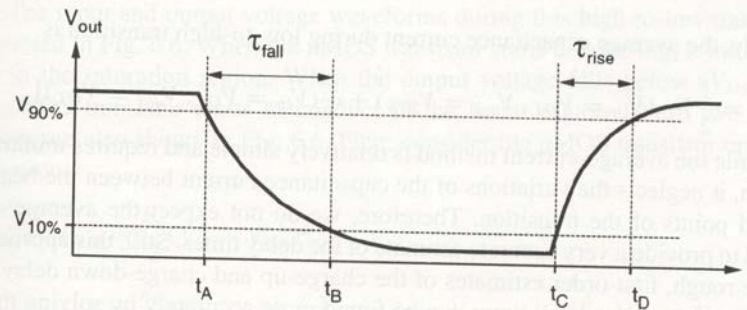
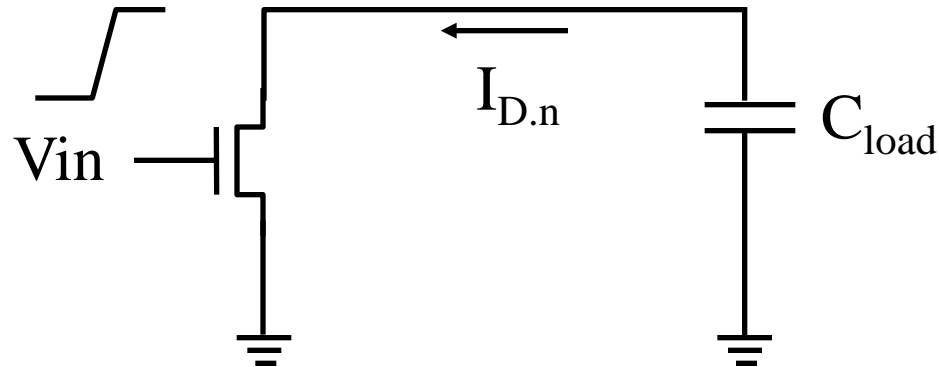


Figure 6.4 Output voltage rise and fall times.

Inverter delay, falling

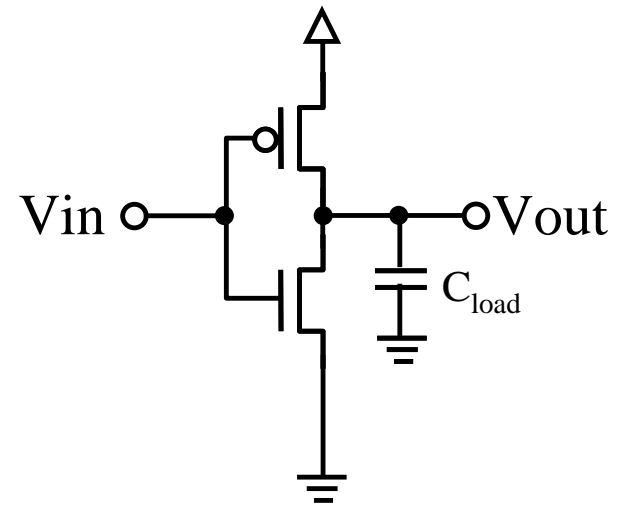


- Assume PMOS fully off ($I_{D,p} = 0$)

$$I = C \frac{dV}{dt}$$

$$I_{D,n} = C_{load} \frac{dV_{out}}{dt}$$

$$dt = C_{load} \frac{dV_{out}}{I_{D,n}}$$



⇒ Need to determine $I_{D,n}$

Calculation of Delay times: Average current method

$$\tau_{PHL} = \frac{C_{load} \cdot \Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load} (V_{OH} - V_{50\%})}{I_{avg,HL}}$$

$$\tau_{PLH} = \frac{C_{load} \cdot \Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load} (V_{50\%} - V_{OL})}{I_{avg,LH}}$$

The average current during high to low transition can be calculated by using the current values at the beginning and the end of the transition.

$$I_{avg,HL} = \frac{1}{2} [i_C(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_C(V_{in} = V_{OH}, V_{out} = V_{50\%})]$$

The average current during low to high transition can be calculated by using the current values at the beginning and the end of the transition.

$$I_{avg,LH} = \frac{1}{2} [i_C(V_{in} = V_{OL}, V_{out} = V_{50\%}) + i_C(V_{in} = V_{OL}, V_{out} = V_{OL})]$$

Average-current method does not provide accurate estimation of delay time

Review: Inverter Delay

Input = High (V_{OH}), NMOS 'on'
and PMOS 'off'

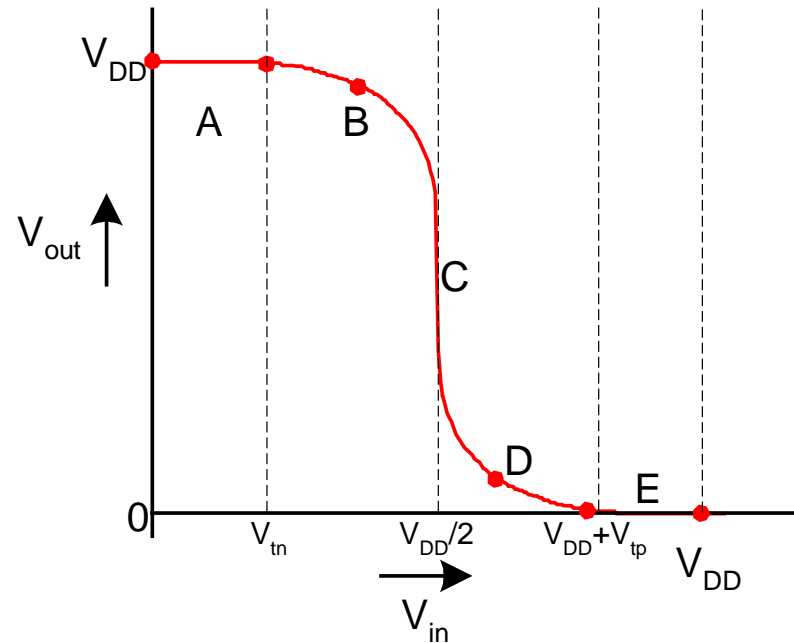
V_{OH} to $V_{OH} - V_{tn}$ → NMOS works
in saturation

$V_{OH} - V_{tn}$ to 0 → NMOS works in
linear region

Input = Low (0), NMOS 'off'
and PMOS 'on'

0 to $|V_{tp}|$ → PMOS works in
saturation

$|V_{tp}|$ to V_{DD} → PMOS works in
linear region



Inverter Delay, falling

$$C_{load} \frac{dV_{out}}{dt} = i_C = i_{D,p} - i_{D,n}$$

$i_{D,p} \approx 0$, for CMOS inverter during H – L transition

$$C_{load} \frac{dV_{out}}{dt} = -i_{D,n}$$

For t_0 to t_1 , NMOS is working in the saturation region

$$i_{D,n} = \frac{k_n}{2} (V_{in} - V_{T,n})^2 = \frac{k_n}{2} (V_{OH} - V_{T,n})^2 \quad \text{for } V_{OH} - V_{T,n} < V_{out} \leq V_{OH}$$

$$\int_{t=t_0}^{t=t_1} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}} \left(\frac{1}{i_{D,n}} \right) dV_{out} = -\frac{2C_{load}}{k_n (V_{OH} - V_{T,n})^2} \int_{V_{OH}}^{V_{OH}-V_{T,n}} dV_{out}$$

$$t_1 - t_0 = \frac{2C_{load} V_{T,n}}{k_n (V_{OH} - V_{T,n})^2}$$

Inverter Delay, falling

For t_1 to t_2 , $V_{out} - V_{T,n}$ to 0 transition, NMOS is working in the linear region

$$i_{D,n} = \frac{k_n}{2} [2(V_{in} - V_{T,n})V_{out} - V_{out}^2] = \frac{k_n}{2} [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2] \text{ for } V_{out} \leq V_{OH} - V_{T,n}$$

$$\int_{t_1}^{t_2} dt = -C_{load} \int_{V_{OH} - V_{T,n}}^{V_{50\%}} \left(\frac{1}{i_{D,n}} \right) dV_{out}$$

$$= -2C_{load} \int_{V_{OH} - V_{T,n}}^{V_{50\%}} \left(\frac{1}{k_n [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2]} \right) dV_{out}$$

$$t_2 - t_1 = -\frac{2C_{load}}{k_n} \frac{1}{2(V_{OH} - V_{T,n})} \ln \left(\frac{V_{out}}{2(V_{OH} - V_{T,n})V_{out} - V_{out}^2} \right) \Bigg|_{V_{OH} - V_{T,n}}^{V_{50\%}}$$

$$t_2 - t_1 = \frac{C_{load}}{k_n (V_{OH} - V_{T,n})} \ln \left(\frac{2(V_{OH} - V_{T,n}) - V_{50\%}}{V_{50\%}} \right)$$

Review: Inverter delay, falling

- Total fall delay =
 $(t_1 - t_0) + (t_2 - t_1)$

$$t_{PHL} = \frac{C_L}{k_n (V_{OH} - V_{T0,n})} \left[\frac{2V_{T0,n}}{V_{OH} - V_{T0,n}} + \ln \left(\frac{4(V_{OH} - V_{T0,n})}{V_{OH} + V_{OL}} - 1 \right) \right]$$

Review: Inverter delay, rising

- ❑ Similar calculation as for falling delay
- ❑ Separate into regions where PMOS is in linear, saturation

$$t_{PLH} = \frac{C_L}{k_p (V_{OH} - V_{OL} - |V_{T0,p}|)} \left[\frac{2|V_{T0,p}|}{V_{OH} - V_{OL} - |V_{T0,p}|} + \ln \left(\frac{4(V_{OH} - V_{OL} - |V_{T0,p}|)}{V_{OH} + V_{OL}} - 1 \right) \right]$$

Review: CMOS inverter actual delay

- What if input has finite rise/fall time? \Rightarrow not a step pulse
 - Both transistors are on for some amount of time
 - Capacitor charge/discharge current is reduced

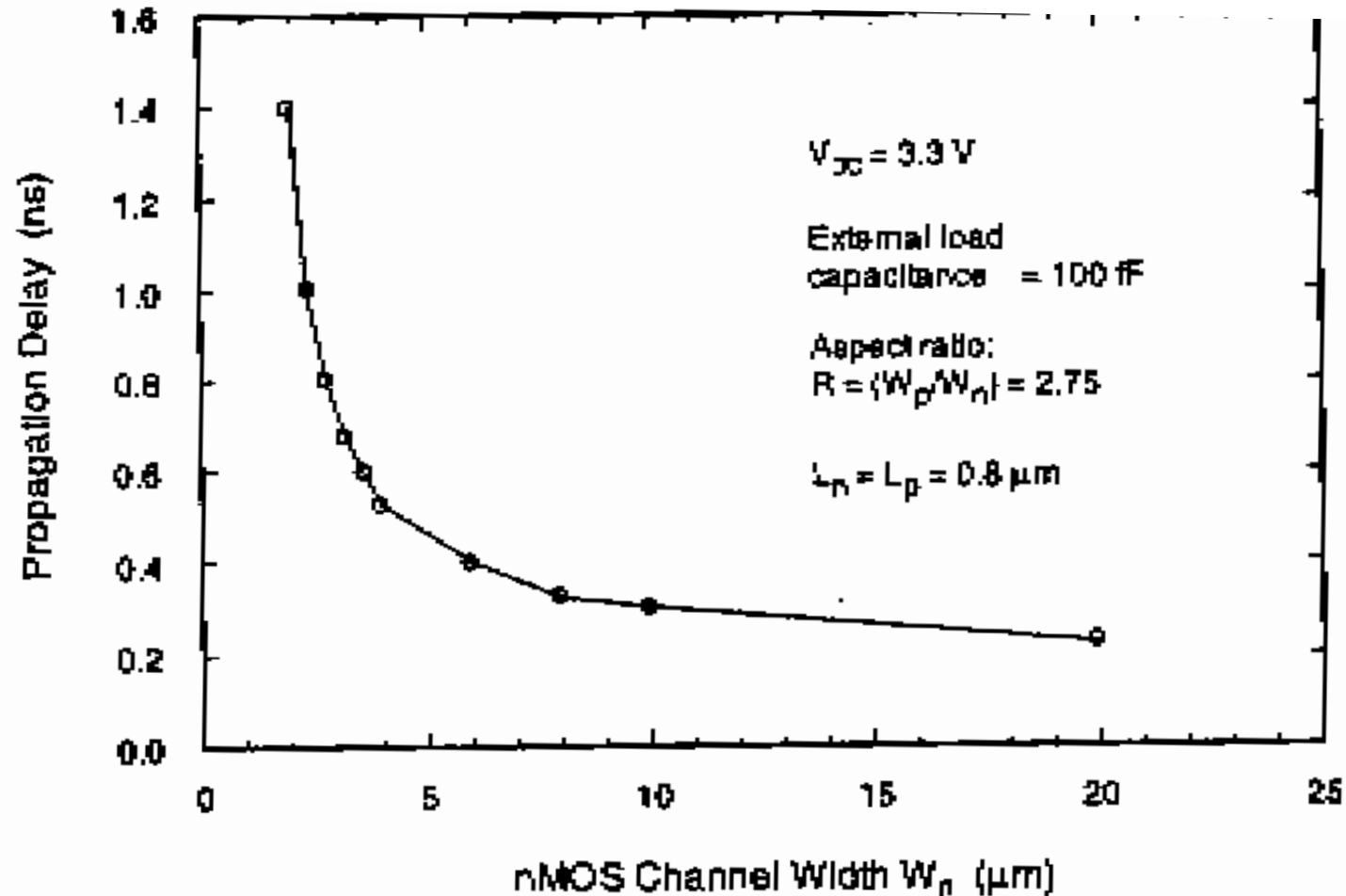
Empirical equations:

$$t_{phl}(actual) = \sqrt{t_{phl}^2(step\ input) + \left(\frac{t_r}{2}\right)^2}$$

$$t_{plh}(actual) = \sqrt{t_{plh}^2(step\ input) + \left(\frac{t_f}{2}\right)^2}$$

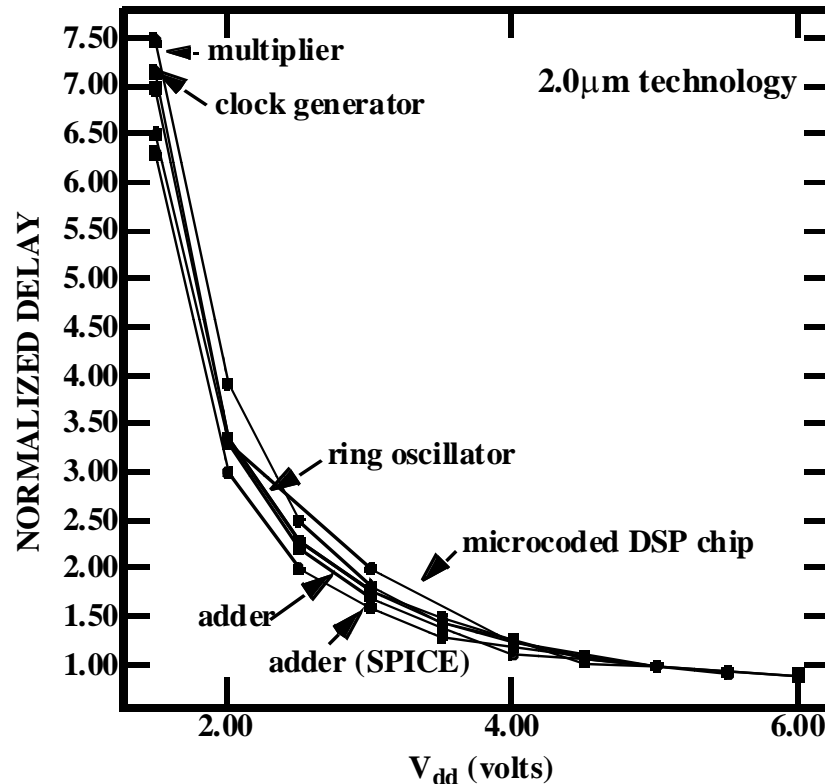
t_r and t_f are the rise time and fall times of the input pulse

Review: Propagation delay simulation results



At very short channel width, the delay approaches a limit value of about 0.2nsec, which is mainly determined by technology-specific parameters, independent of extrinsic capacitance component.

Review: Inverter delay revisited (Lower V_{dd} Increases Delay)



$$T_d = \frac{C_L * V_{dd}}{I}$$

$$I \sim (V_{dd} - V_t)^2$$

$$\frac{T_d(V_{dd}=2)}{T_d(V_{dd}=5)} = \frac{(2) * (5 - 0.7)^2}{(5) * (2 - 0.7)^2} \approx 4$$

- Relatively independent of logic function and style.

CMOS Ring Oscillator Circuit

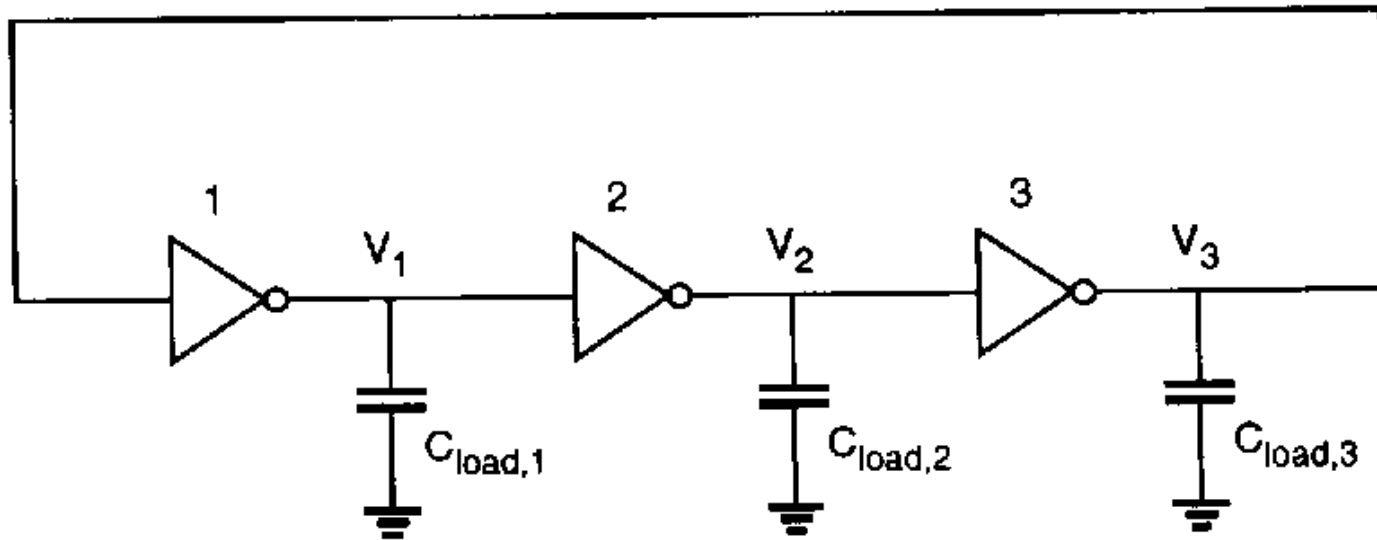


Figure 6.9 Three-stage ring oscillator circuit consisting of identical inverters.

CMOS Ring Oscillator Circuit (cont.)

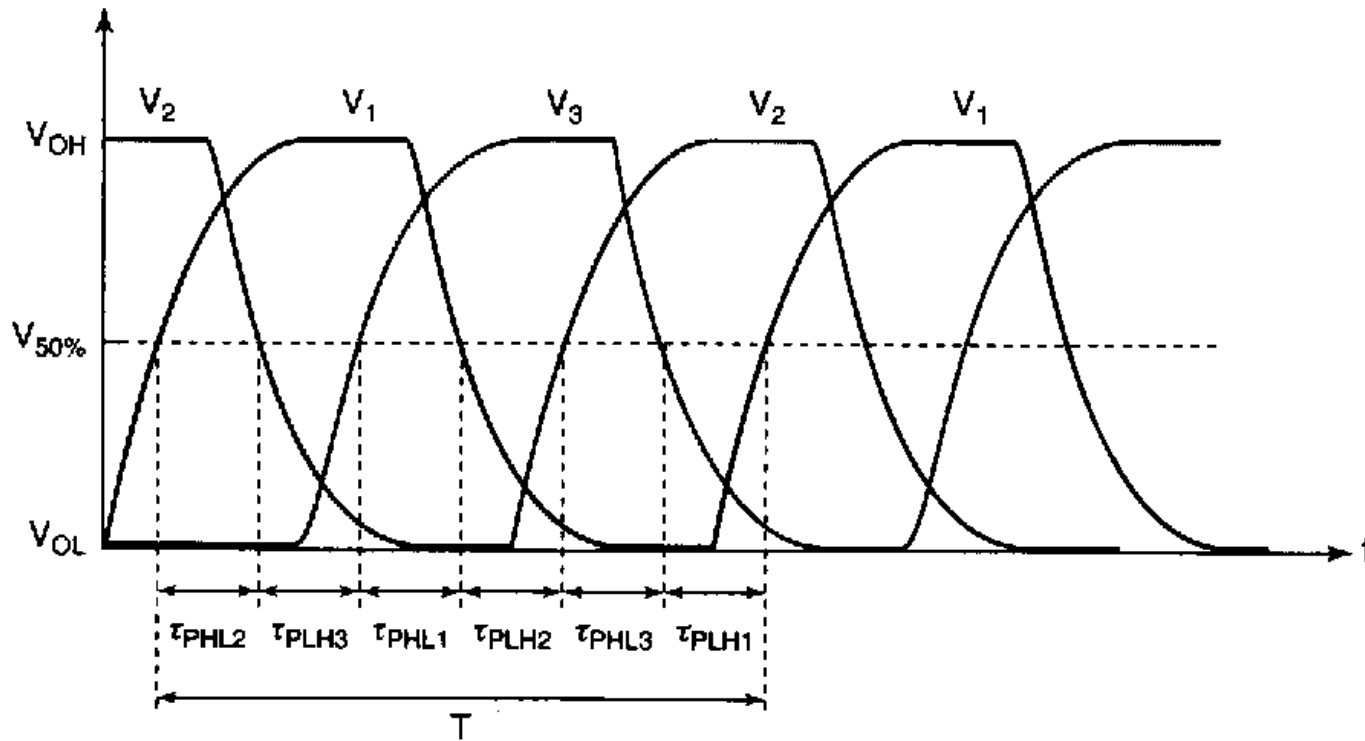


Figure 6.10 Typical voltage waveforms of the three inverters shown in Fig. 6.9.

$$\begin{aligned}
 T &= \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3} \\
 &= 2\tau_p + 2\tau_p + 2\tau_p \\
 &= 6\tau_p
 \end{aligned}$$

$$f = \frac{1}{T} = \frac{1}{2n\tau_p}$$

$$\tau_p = \frac{1}{2nf}$$

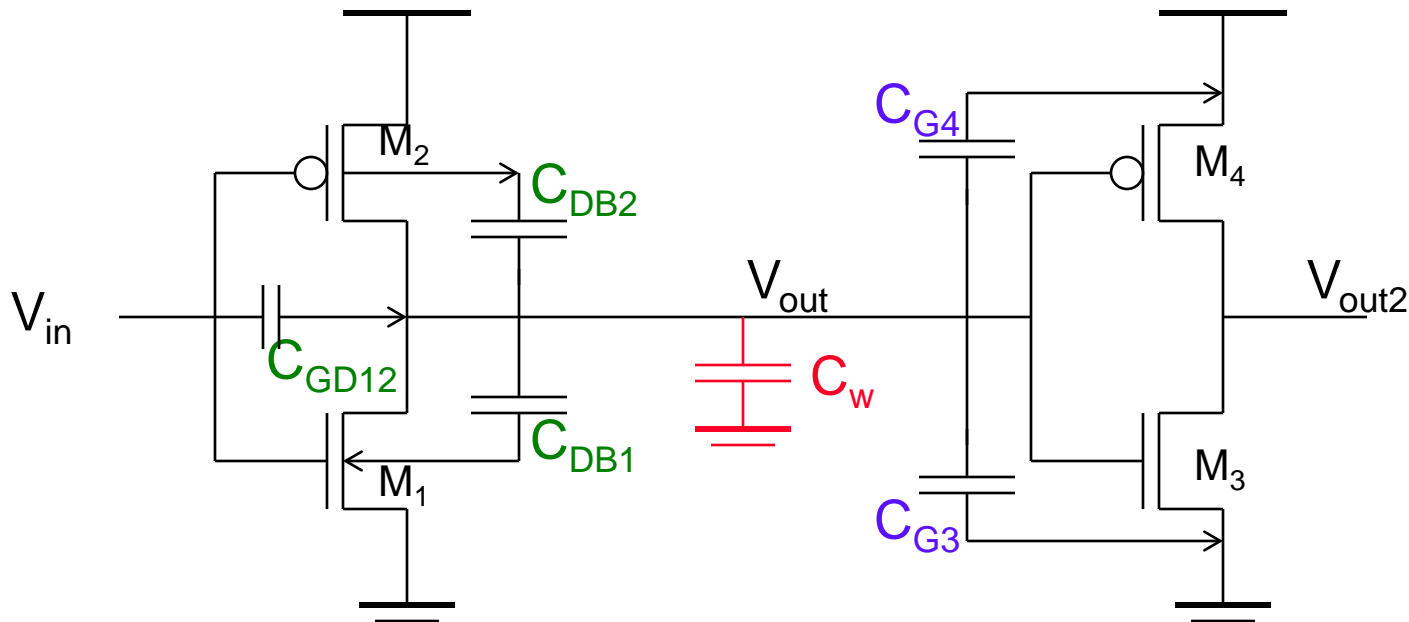
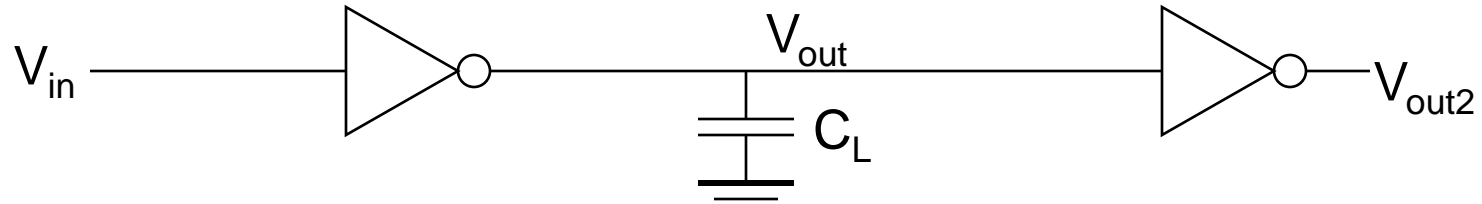
Delay Estimation

Switching speed of logic gate is based on the assumption → load is capacitive and lumped

Conventional delay estimation has mainly three contributing factors

- (1) internal parasitic capacitance of the transistors
- (2) interconnect line capacitance
- (3) input capacitances of the fan-out gates

Sources of Capacitance



intrinsic MOS transistor capacitances

extrinsic MOS transistor (fanout) capacitances

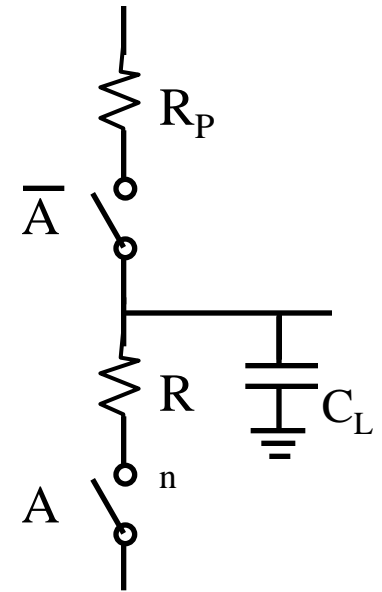
wiring (interconnect) capacitance

Calculation of interconnect delay: Switch-level model (RC delay model)

- ❑ Model transistors as switches and resistances
- ❑ Resistance R_{on} = average resistance for a transition
- ❑ For NMOS t_{phi} :

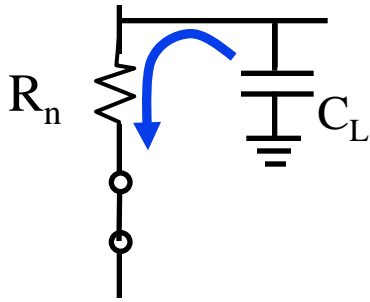
$$R_{on} = \frac{1}{2} \left(R_{NMOS}(V_{out} = V_{CC}) + R_{NMOS}(V_{out} = \frac{1}{2}V_{CC}) \right)$$

$$R_{on} = \frac{1}{2} \left[\left(\frac{V_{DS}}{I_D} \right)_{V_{out}=V_{CC}} + \left(\frac{V_{DS}}{I_D} \right)_{V_{out}=\frac{1}{2}V_{CC}} \right]$$



Switch-level model

Delay estimation using switch-level model (for general RC circuit):



$$I = C \frac{dV}{dt} \quad \rightarrow \quad dt = \frac{C}{I} dV$$

$$I = \frac{V}{R} \quad \rightarrow \quad dt = \frac{RC}{V} dV$$

$$t_1 - t_0 = t_p = \int_{V_0}^{V_1} \frac{RC}{V} dV$$

$$t_p = RC [\ln(V_1) - \ln(V_0)] = RC \ln\left(\frac{V_1}{V_0}\right)$$

Propagation delay of simple lumped RC network

- For fall delay t_{phl} , $V_0 = V_{CC}$, $V_1 = V_{CC}/2$

$$t_p = RC \ln\left(\frac{V_1}{V_0}\right) = RC \ln\left(\frac{\frac{1}{2}V_{CC}}{V_{CC}}\right)$$

$$t_p = RC \ln(0.5)$$

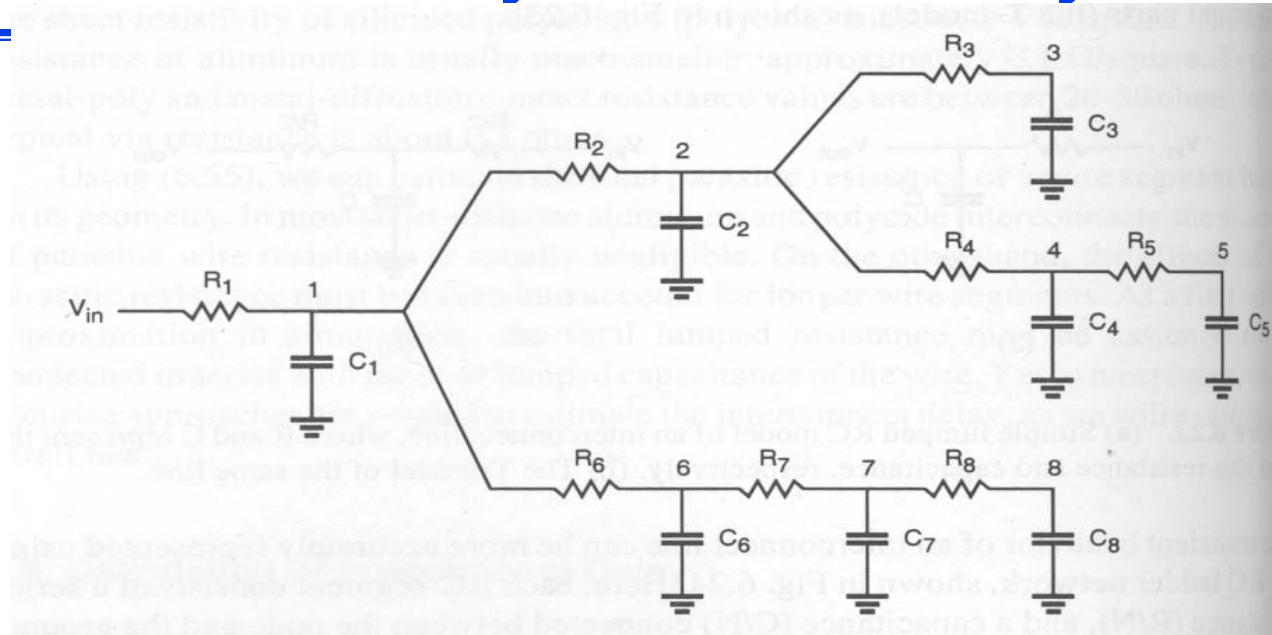
$$t_{phl} = 0.69R_n C_L$$

$$t_{plh} = 0.69R_p C_L$$

Standard RC-delay
equations



Interconnect delay – Elmore Delay



- ❑ For long interconnect lines, RC must be distributed to obtain accurate simulation results
- ❑ Elmore Delay – first order time constant
 - simple, close approximation of delay

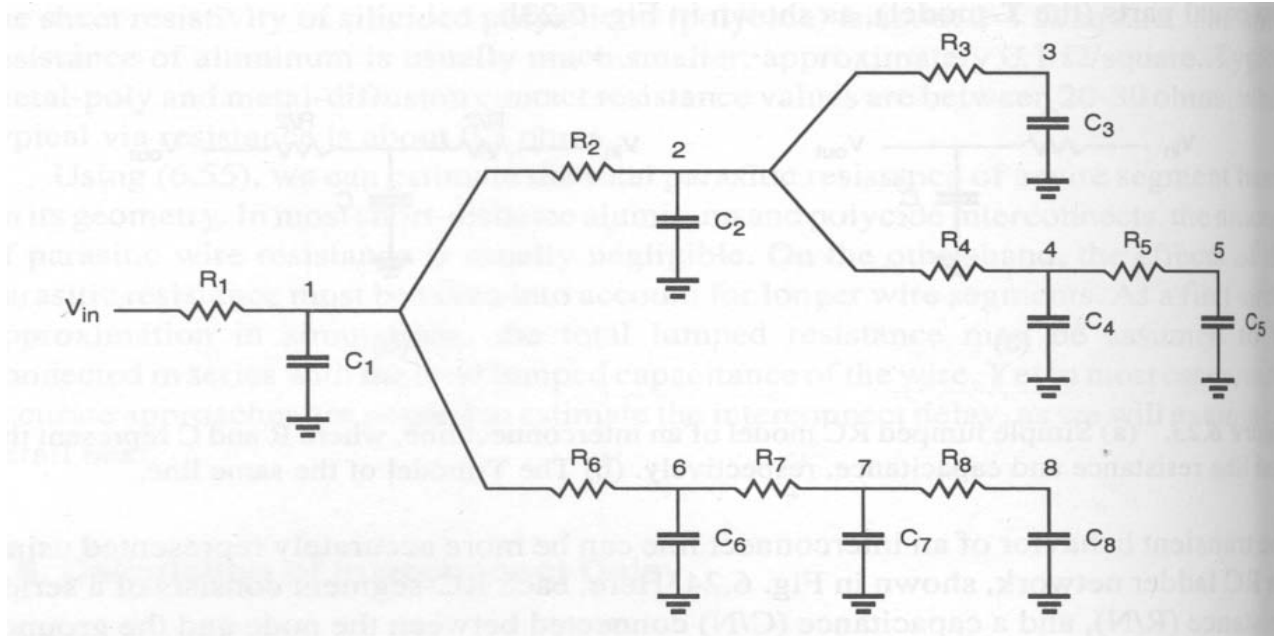
$$\tau_{Di} = \sum_{j=1}^N C_j \sum_{k \in p_{ij}} R_k$$

$P_i \rightarrow$ unique path from input to node i
 $P_{ij} = P_i \cap P_j \rightarrow$ common path between P_i and P_j

N = number of capacitors

R_k = resistance seen by each capacitor

Interconnect delay – Elmore Delay



Elmore delay at node 7 $\tau_{D7} = R_1 C_1 + R_1 C_2 + R_1 C_3 + R_1 C_4 + R_1 C_5 + (R_1 + R_6) C_6 + (R_1 + R_6 + R_7) C_7 + (R_1 + R_6 + R_7) C_8$

Elmore delay at node 5

$$\tau_{D5} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2) C_3 + (R_1 + R_2 + R_4) C_4 + (R_1 + R_2 + R_4 + R_5) C_5 + R_1 C_6 + R_1 C_7 + R_1 C_8$$

Interconnect Resistance

$$R_{wire} = \rho \frac{l}{A} = \rho \frac{l}{wt} = R_{sheet} \frac{l}{w}$$
$$\rho(\text{resistivity}) = \Omega m$$

- Resistance is proportional to cross-sectional area
 - As interconnect scales, increase aspect ratio to maintain same area.

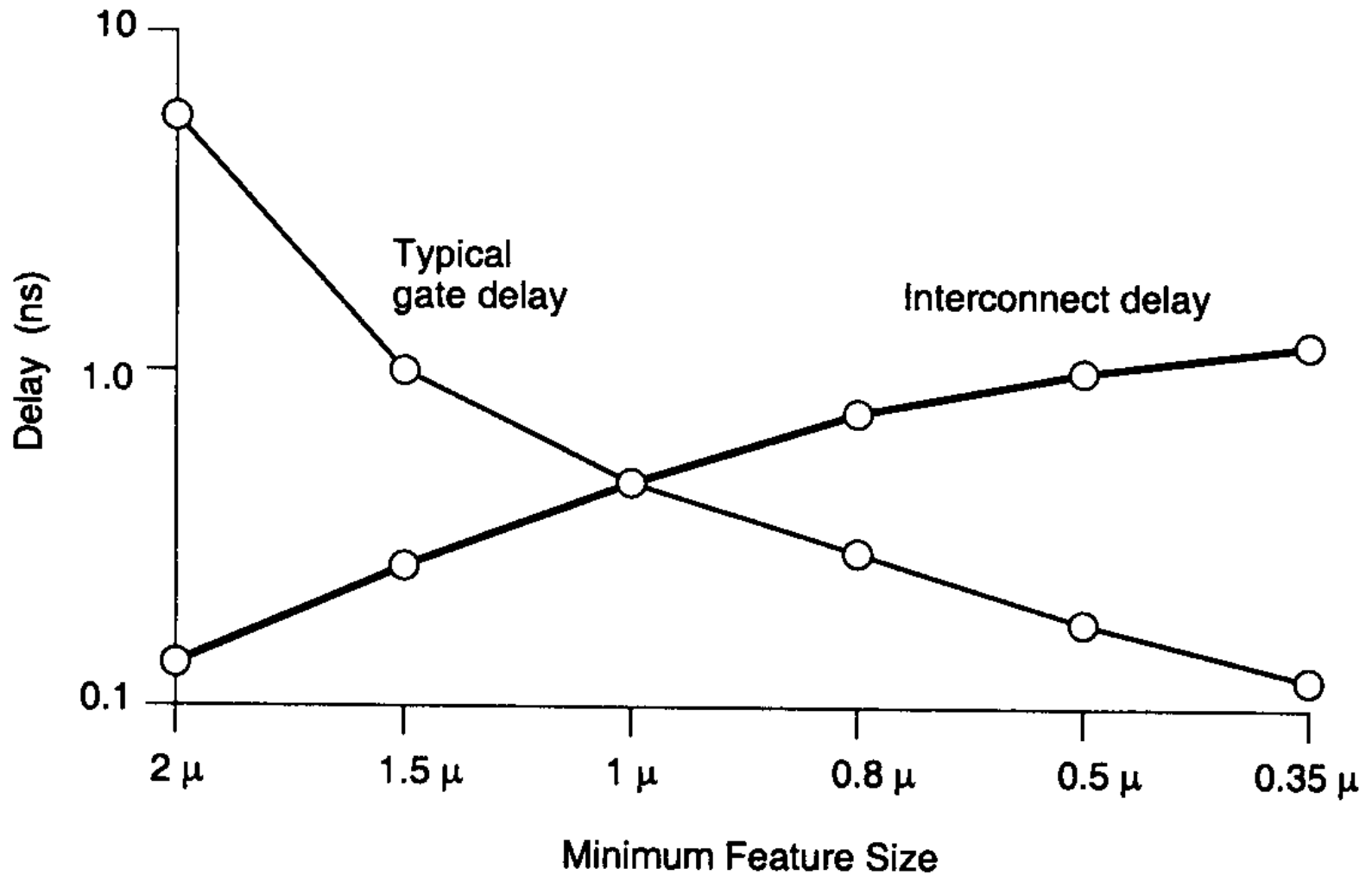


Figure 6.13 Interconnect delay dominates gate delay in sub-micron CMOS technologies.

Review: Designing Inverters for Performance

□ Reduce C_L

- internal diffusion capacitance of the gate itself
- interconnect capacitance
- fanout

□ Increase W/L ratio of the transistor

- the most powerful and effective performance optimization tool in the hands of the designer

□ Increase V_{DD}

- only minimal improvement in performance at the cost of increased energy dissipation

□ Slope engineering - keeping signal rise and fall times smaller than or equal to the gate propagation delays and of approximately equal values

- good for performance
- good for power consumption