

ES330 Laboratory Prof. S. Saraf

Lab 5: MOSFET Current Sources

Objective

The current source ideally provides constant DC bias current for amplifier stages and is a fundamental building block in electronic design. This lab project will investigate the use of MOSFETs to design current sources.

Theory

The operation of the MOSFET current source is dependent on the MOSFET device parameters and on the load being driven by the current source. The basis of most current sources is the current mirror shown in Figure 1. We will assume that the NMOS transistors M_1 and M_2 used in this current mirror are matched, which means that the transistors have the same threshold voltage V_t , channel width W , channel length L , and $k'_n = \mu_n C_{ox}$, where μ_n is the effective electron mobility in the n-channel and C_{ox} is oxide capacitance per unit area. The connection of the transistors in Figure 1 ensures that the gate-to-source voltage V_{GS} for each transistor is the same. Therefore, the drain current I_{D1} is the same as the drain current I_{D2} . Also notice that the current I_{REF} is equal to I_{D1} , since the gate terminals do not draw any DC current. In other words, the drain current $I_{D2} = I_{OUT}$ should mirror the reference current, I_{REF} , to a good first approximation.

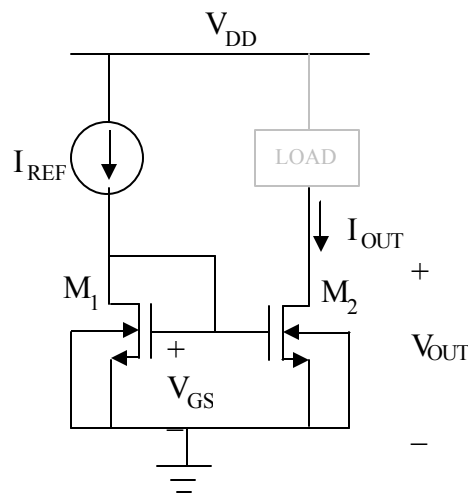


Figure 1. Simple current mirror

Ideally, the output current I_{D2} , should be constant regardless of the load used. Realistically, I_{D2} is dependent upon the drain-to-source voltage, V_{DS} , of M_2 , as shown by the following equations:

$$i_D = k_n' \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right], \quad v_{DS} \leq v_{GS} - V_t$$

$$= \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \mathbf{I} (v_{DS} - v_{DSsat})), \quad v_{DS} \geq v_{GS} - V_t$$

where \mathbf{I} is the channel length modulation parameter and $v_{DSsat} = v_{GS} - V_t$.

An alternate design for the MOSFET constant current source is the modified Wilson current source shown in Figure 2. Note that all body connections go to ground. Since we are using a separate chip for M_2 / M_4 than we are for M_1 / M_3 , we *could* eliminate body effect in M_2 and M_4 by connecting their bodies directly to their sources. However, that is not realistic because — in an integrated circuit — all the NMOS substrates (bodies) are common, tied to the lowest potential in the circuit. (Also, all the PMOS substrates (bodies) are common, tied to the highest potential in the circuit.)

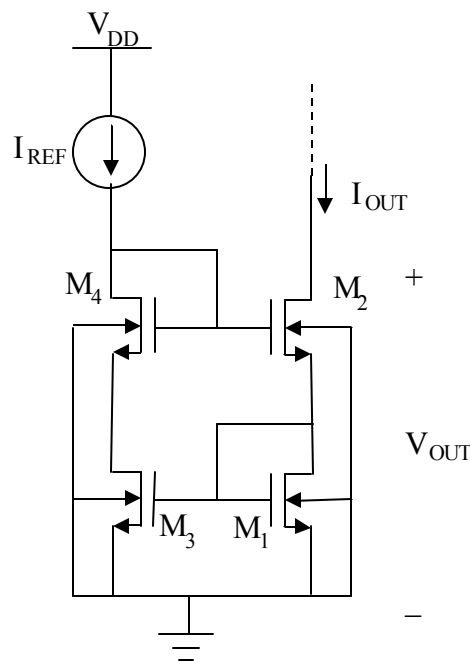


Figure 2. Modified Wilson current source

The advantage of the Wilson current source over the simple current mirror is in the output impedance of the current source. An analysis of the small signal equivalent circuit of each source shows the output impedance of the simple current source to be the small-signal output impedance of transistor M_2 :

$$R_{out(simple)} = r_o$$

For the Wilson current source, the output impedance is increased essentially by the factor $(g_m r_o)$. This factor can be shown to be in the range of 20 to 100; thus the increase in the output resistance of a Wilson current source structure is significant.

$$R_{out(Wilson)} = (g_m r_o) r_o = g_m r_o^2$$

(It should be noted that a careful derivation of the output resistance gives several additional terms that are of the order of r_o in magnitude. The result above is the dominant term in the analysis.) We could have achieved the same output impedance without using the fourth transistor M_4 , in which case this circuit becomes a Wilson current source instead of a modified Wilson current source. However, in the case of modified Wilson current source, the drain voltages of M_1 and M_3 are equal and thus their currents will be equal.

The output impedance provides a measure of how sensitive the current source is to variations in the load. The output impedance of an ideal current source is infinite, so the Wilson current source should provide better overall performance than the simple current mirror.

(Note, however, that there is a disadvantage to stacking devices as in the modified Wilson current source: every device must be kept in saturation in order to operate properly for analog purposes, and that implies that at least V_{DSsat} must be maintained across every device. With a fixed amount of voltage available from the upper to the lower power supply, using more of it in a stacked current source leaves less for the load itself.)

MOSFET current mirrors are also useful in providing a simple way of generating multiple currents for different stages of a circuit. The output current can be scaled by scaling the W/L ratio appropriately. An example of a two-output MOSFET current source is shown in Figure 3.

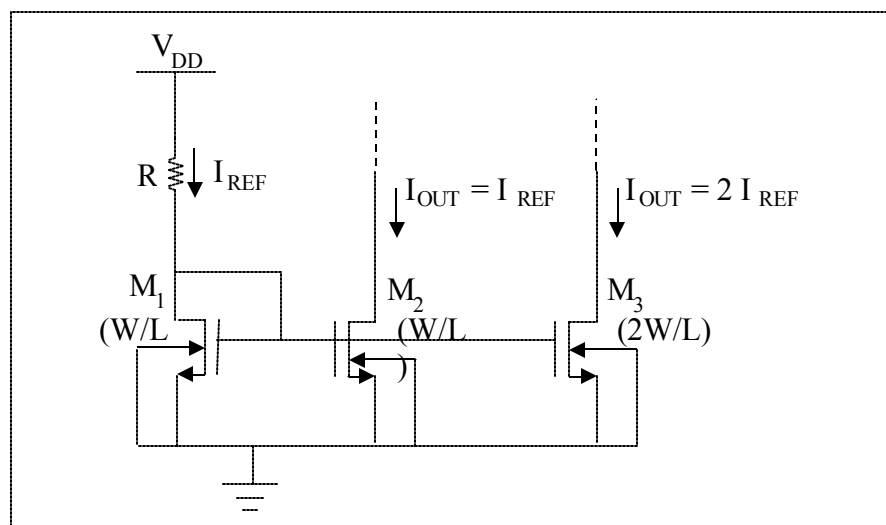


Figure 3. Two-output MOSFET current source

This lab will use an NMOS matched pair contained in the ALD1103 chip. You will need two such chips for the Wilson source. Refer to the data sheet given in the previous lab for the chip pin-out. Pay particular attention to the substrate connections for the NMOS devices, pin **4**.

Note that there are two NMOS and two PMOS devices on each chip. The p -substrate connection (pin **4**) is common to the two NMOS devices; the n -substrate connection (pin **11**) is common to the two PMOS devices.

Pre-Lab

- (1) Derive the small-signal model output impedance, R_{out} , of the simple and modified Wilson current sources. Assume that the NMOS devices in a single ALD1103 package are matched to each other. Start by drawing the small-signal equivalent circuit. It is reasonable to replace any diode-connected transistor with its equivalent resistance, $1/g_m$. Do not include the body-effect generator, $g_{mb} v_{sb}$, in the MOSFET model— it will needlessly complicate your analysis here.
 - (2) Design the simple current mirror and the modified Wilson current source for a 4 mA dc drain current by selecting an appropriate value of resistance R to replace the ideal I_{REF} source. Note that you will have to round your calculated value to a standard resistor value. *Note also that the required resistance values will be different for the two different sources.* Use $V_{DD} = 5.0$ V for the simple current mirror and $V_{DD} = 10.0$ V for the modified Wilson current source. Assume that $V_{Tn} \sim 0.7$ V, the NMOS intrinsic transconductance is $k'_n = 25 \mu\text{A}/\text{V}^2$, and W/L for all devices is 100:1.
 - (3) For both the simple current mirror and the modified Wilson current source, calculate the value of the load resistance that will drive the output transistor of the current source out of saturation. (They will be different values.) These would be the *maximum* load resistances that could be used and still have the current sources operate properly.
 - (4) Simulate the simple current mirror and the modified Wilson current source for a range of load resistances (up to the maximum values calculated previously) using PSPICE.
 - ⇒ Note that the load resistance should be connected between the output node and V_{DD} .
 - ⇒ Note that all NMOS substrates must be connected to the lowest potential (ground, here).
 - ⇒ Make sure that you edit and modify the *MbreakN* (NMOS) model to include parameters that apply to all ALD1103 NMOS devices: $V_{Tn} = 0.7$ V, intrinsic transconductance $k'_n = 25 \mu\text{A}/\text{V}^2$, $I_n = 0.02 \text{ V}^{-1}$, $\gamma = 0.9 \text{ V}^{1/2}$, $t_{ox} = 90$ nm, $N_{sub} = 3.7 \times 10^{15} \text{ cm}^{-3}$, version = 2 (PSPICE parameters VTO, KP, LAMBDA, GAMMA, TOX, NSUB, VERSION).
- ⇒ Also remember to set the appropriate size for each individual device: $W = 1000 \mu\text{m}$, $L = 10 \mu\text{m}$ for $W/L = 100:1$.
- ⇒ Use $V_{DD} = 5.0$ V for the simple current mirror and $V_{DD} = 10.0$ V for the modified Wilson current source.
- ? Observe the output currents and their dependence on the varying load resistance.
 - ? Verify that the maximum tolerable load resistance is approximately correct.
- (5) Using the basic current mirror design, simulate a multiple output current mirror with two output transistors as shown in Figure 3.

- ⇒ Make sure you set the W and L properly for M_3 , the double-wide device.
- ⇒ Note that all NMOS substrates must be connected to the lowest potential (ground, here).
- ? Measure and compare the reference and output currents to those in the basic current mirror.

Lab Exercise

- (1) Use one ALD1103 package to build the circuit in Figure 1, replacing the ideal current source I_{REF} with the resistor value that you calculated in your pre-lab work. The pin diagram for the ALD1103 is shown in the data sheet (Figure 4).
 - ⇒ Note that all NMOS substrates must be connected to the lowest potential (ground, here).
 - ⇒ Vary the load resistance connected between the output node (the drain of M_2) and V_{DD} to generate different drain-to-source voltages. Recall from your pre-lab calculations and simulations that there is a maximum value of load resistance that should not be exceeded.
 - ? For each load resistance, measure the reference and output currents, I_{REF} and I_{OUT} , respectively, as well as the output voltage (V_{DS} of M_2). Take measurements for at least six different values of load resistance.

- (2) Build the circuit in Figure 3 by modifying the simple current mirror.
 - ⇒ To get a transistor with $2W/L$, connect the two NMOS devices from a second ALD1103 package in parallel — *i.e.*, wire the two drains together; wire the two sources together; wire the two gates together; the two substrates are already wired together internally.
 - ⇒ Don't forget about the substrate connection in the second ALD1103 package (pin 4).
 - ⇒ Note that all NMOS substrates must be connected to the lowest potential (ground, here).
 - ⇒ Vary the load resistance connected between the output nodes (the drains of M_2 and M_3) and V_{DD} to generate different drain-to-source voltages. Use the **same** resistor value for both output nodes.
 - ? Measure the reference current and both output currents, as well as the output voltages (V_{DS} of M_2 and M_3). Take measurements for at least six different values of load resistance.

- (3) Use two ALD1103 packages to build the modified Wilson circuit in Figure 2, replacing the ideal current source I_{REF} with the resistor value that you calculated in your pre-lab work.
 - ⇒ Note that all NMOS substrates must be connected to the lowest potential (ground, here).
 - ⇒ Vary the load resistance connected between the output node (the drain of M_2) and V_{DD} to generate different drain-to-source voltages. Recall from your pre-lab calculations and simulations that there is a maximum value of load resistance that

should not be exceeded.

? For each load resistance, measure the reference and output currents, I_{REF} and I_{OUT} , respectively, as well as the output voltage (V_D of M_2). Take measurements for at least six different values of load resistance.

Analysis of results

For the simple current source:

- (1) Tabulate your measured reference and output currents, as well as the output voltages, for each resistor value.
- (2) Plot V_{DS} vs. I_o and determine R_{out} as the gradient (slope). (An approximate alternative: Going two data points at a time, calculate the apparent R_{out} of your current source as $R_{out} = \Delta V_{DS} / \Delta I_o$. Include the R_{out} values in your table.)
- (3) Compare your calculated R_{out} value(s) to the theoretical value for this current source topology. Use $\lambda = 0.02 \text{ V}^{-1}$ for your theoretical calculation.

For the modified Wilson current mirror:

- (1) Tabulate your measured reference and output currents, as well as the output voltages, for each resistor value.
- (2) Plot V_o vs. I_o and determine R_{out} as the gradient (slope). (An approximate alternative: Going two data points at a time, calculate the apparent R_{out} of your current source as $R_{out} = \Delta V_o / \Delta I_o$. Include the R_{out} values in your table.)
- (3) Compare your calculated R_{out} value(s) to the theoretical value for this current source topology. Use $\lambda = 0.02 \text{ V}^{-1}$ for your theoretical calculation.

For the multiple-output current source:

- (1) Compare the output current from the output transistor with W/L to the output current from the output transistor with $2W/L$.
- (2) Explain why the current from the $2W/L$ “device” is not twice the current from the W/L device.