

ES330 Laboratory Prof. S. Saraf

Lab 6: MOSFET Differential Pair with Resistive Load

Overview

The differential amplifier is a fundamental building block in electronic design. The objective of this lab is to examine the voltage transfer characteristic and performance of a MOSFET differential amplifier with resistive loads — *i.e.*, with resistors R_D connected from the drain terminals of the MOSFETs to the positive power supply.

Theory

Introduction:

The differential amplifier is a two-input/two-output circuit, as shown in Figure 1. In this lab, the amplifier will be examined in a single-ended configuration, taking the output as v_{o1} or v_{o2} . The two inputs of the differential amplifier are at the gates of M_1 and M_2 . When these inputs are grounded, the bias current available from the current source, I_o , splits evenly between the two transistors, assuming that the transistors are identical. The corresponding voltage between the gate and source of the two transistors is known as the Q point voltage (V_{GSQ}).

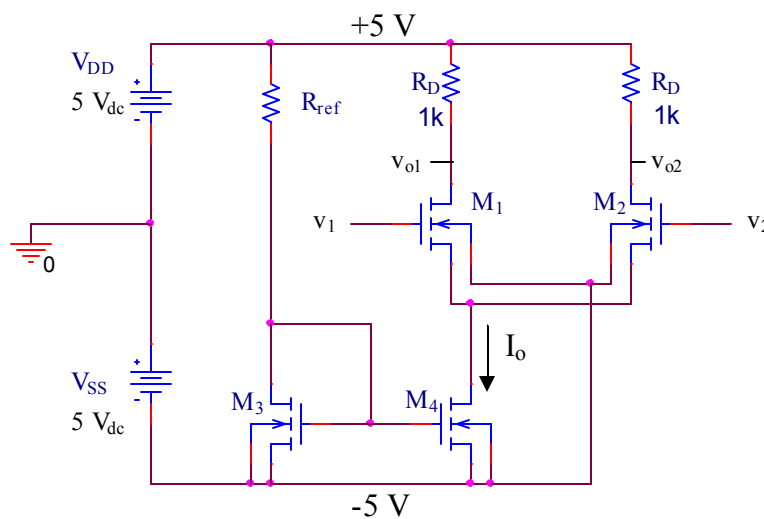


Figure 1. Differential amplifier with resistive load

DC Voltage Transfer Characteristics of a Differential Amplifier:

When a differential mode input signal v_{diff} is connected to the differential amplifier — that is, when one input is set at $\left(+\frac{v_{diff}}{2}\right)$ and the other is set at $\left(-\frac{v_{diff}}{2}\right)$ — the current in one transistor increases while the current in the other decreases. The drain voltage v_{o1} of M_1 will decrease (or increase) from its Q point value depending on whether v_{diff} is positive (or negative). If the input signal is sufficiently positive, then v_{o1} will reach a minimum value and saturate at that value. If the input signal is sufficiently negative, then v_{o1} will reach a maximum value of V_{DD} and saturate at that value. If the input signal to M_1 is started at a sufficiently large negative value of v_{diff} and gradually increased toward a sufficiently positive value of v_{diff} , the voltage v_{o1} starts initially at a constant value of V_{DD} , then goes through a segment where v_{o1} is proportional to v_{diff} , and then saturates at a minimum value given by $(V_{DD} - R_D I_o)$. The region where v_{o1} is proportional to v_{diff} is used in analog amplification.

Differential Mode Operation:

Figure 2 shows the differential amplifier with inputs applied in differential mode. Assuming matched transistors, the following equations describe the gain of the amplifier.

With $v_1 = +\frac{v_{diff}}{2}$ and $v_2 = -\frac{v_{diff}}{2}$, the differential mode gains $\left(\frac{v_{o1}}{v_{diff}}\right)$ of a differential amplifier are given by Equations (1) and (2):

$$A_{d1} = \left(\frac{v_{o1}}{v_{diff}}\right) = -\frac{1}{2} g_m (R_D \parallel r_o \parallel R_L) \quad (1)$$

$$A_{d2} = \left(\frac{v_{o2}}{v_{diff}}\right) = \frac{1}{2} g_m (R_D \parallel r_o \parallel R_L) \quad (2)$$

where g_m is given by

$$g_m = m_n C_{ox} \left(\frac{W}{L}\right) (V_{GSQ} - V_t) = k_n' \left(\frac{W}{L}\right) (V_{GSQ} - V_t) = \sqrt{2k_n I_D} = \sqrt{2k_n \left(\frac{I_o}{2}\right)} \quad (3)$$

where I_D is the DC current in M_1 or M_2 , and where a load resistance R_L may be attached to the output node (not shown in figure). If R_L is not included, we would let $R_L = \infty$ in Equations (1) and (2).

Note that — in principle — a common-mode DC supply (V_{com}) must be provided in addition to the differential signal to bias the amplifier in the correct operating region (all transistors in saturation). This ensures that we get undistorted, or linear, amplification. Since the lower power supply is at -5 V, a value of $V_{com} = 0$ V may be sufficient, but this should be checked as part of the pre-lab preparation.

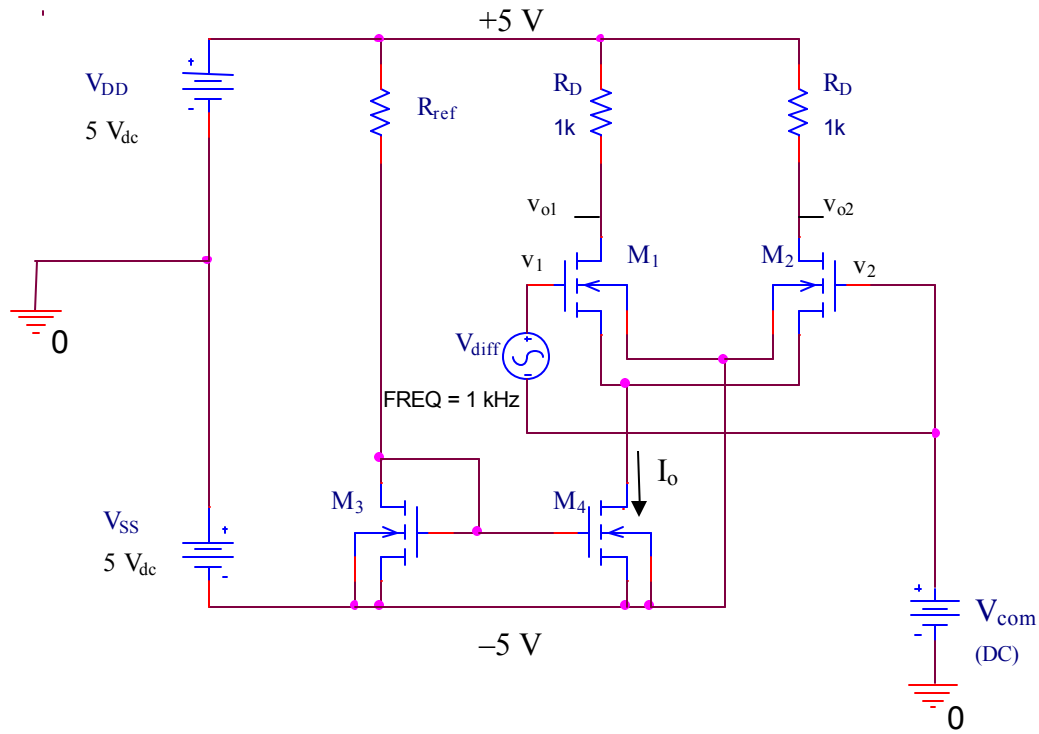


Figure 2. Differential amplifier in differential mode

Common Mode Operation:

Figure 3 shows the differential amplifier with inputs applied in common mode. With v_1

$= v_2 = v_{CM}$, the common mode gain $\left(\frac{v_{o1}}{v_{CM}} \right)$ is given by

$$A_{CM} = \left(\frac{v_{o1}}{v_{CM}} \right) = \left(\frac{v_{o2}}{v_{CM}} \right) = -\frac{g_{m1}(R_D \parallel R_L)}{1 + 2g_{m1}R_o} = -\frac{g_{m2}(R_D \parallel R_L)}{1 + 2g_{m2}R_o} \quad (4)$$

where R_o is the output resistance of the current source. For a simple current source,

$$R_o = r_{o4} \approx \frac{1}{II_o} \quad (5)$$

Common Mode Rejection Ratio:

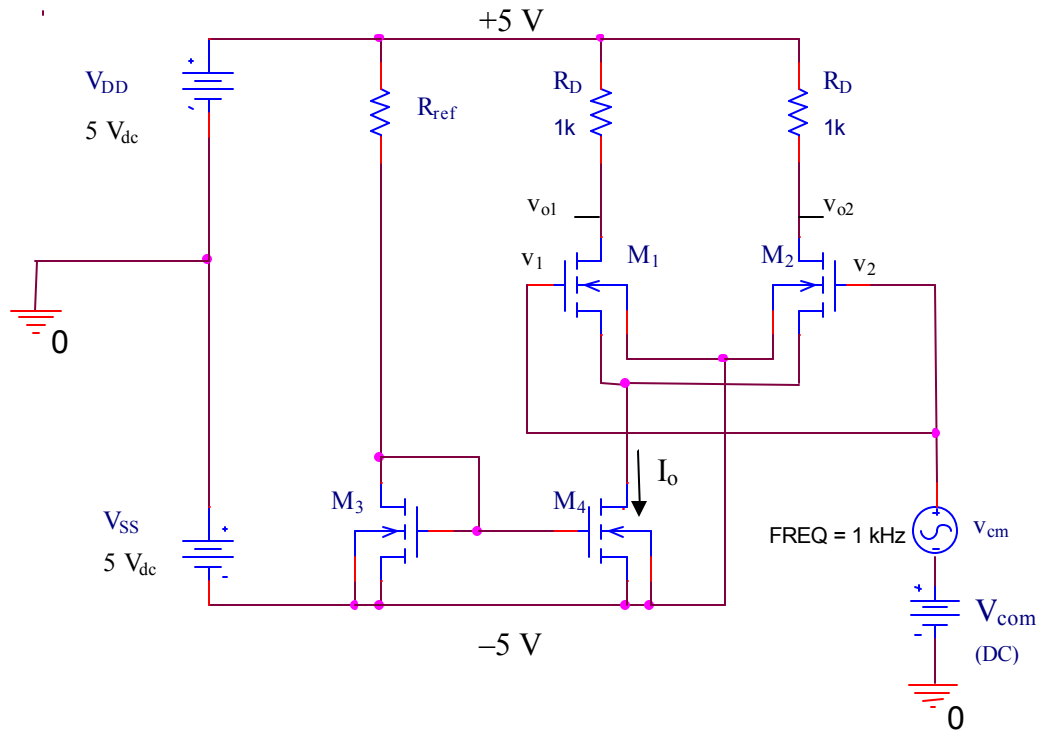


Figure 3. Differential amplifier in common mode

Pre-Lab

Assume the following device parameters:

$V_t = 0.7$ V, $k'_n = 25$ $\mu\text{A}/\text{V}^2$, $I_n = 0.02$ V^{-1} , $\gamma = 0.9$ $\text{V}^{1/2}$, $t_{ox} = 90$ nm, $N_{sub} = 3.7 \times 10^{15}$ cm^{-3} , version = 2 (PSPICE parameters VTO, KP, LAMBDA, GAMMA, TOX, NSUB, VERSION), and $W/L = 100/1$.

- (1) Design the M_3 – M_4 simple current source to provide a 4 mA drain current in M_4 by calculating and selecting the correct value for R_{ref} . *Note: Standard resistor value(s) should be used for R_{ref} since these will be used during the hardware portion of the lab.*
- (2) Assuming a 4 mA drain current through M_4 , calculate the theoretical Q point values by grounding both inputs of the amplifier in Figure 1 and finding V_{GSQ1} and V_{GSQ2} .
- (3) A DC common mode voltage (V_{com}) will be required to allow bias current to flow in the complete differential amplifier circuit. Calculate the minimum value of V_{com} that can be applied and still ensure proper operation (*i.e.*, all transistors in saturation) of the differential pair.
- (4) Using the Q point values calculated in part (2), calculate the theoretical differential mode gain, common mode gain, and common mode rejection ratio (CMRR) at v_{o1} and v_{o2} .
- (5) Use PSPICE to obtain simulation values for the Q point voltages. Use the *MbreakN / BREAKOUT* component for the NMOS devices, editing and modifying their properties to be consistent with the actual devices we are using. Refer to Labs #1 and #2 for guidance in editing the model properties.
- (6) Use PSPICE to simulate the Voltage Transfer Characteristic (VTC). A *DC sweep* input can be used to determine the VTC, sweeping the range of v_{diff} from -5 V to $+5$ V, with increments of 0.1 V.
- (7) Simulate the circuit in Figure 2 with four different input values of v_{diff} to find the differential mode gain at v_{o1} and v_{o2} . Use an input range of 500 mV(pp) to 2 V(pp) at a frequency of 1 kHz for v_{diff} .
- (8) Simulate the circuit in Figure 3 with four different input values of v_{cm} to find the common mode gain at v_{o1} and v_{o2} . Use an input range of 1 V(pp) to 3 V(pp) for v_{cm} at a frequency of 1 kHz. Calculate the common mode rejection ratio of the amplifier.

Objectives:

- (1) To obtain the voltage transfer characteristics of a MOSFET differential pair with differential mode inputs.
- (2) To measure the differential mode gain and common mode gain, and to determine the CMRR.

Hardware Procedure:

- ** The NMOS substrate (pin 4) must be connected to the most negative voltage supply (–5 V here). Also remember to apply power to V_{DD} and V_{SS} before connecting the input signals to the gates of M_1 and M_2 , and remove the input signals before disconnecting power. Refer to the pin-out diagram in the data sheet given as Figure 4.
- ** Make sure the signal generator is in High Z mode.
- ** Using cursors may help avoid noise in oscilloscope autoscaling.

- (1) Two ALD 1103 packages will be used. Using the R_{ref} value calculated previously, build the differential amplifier circuit shown in Figure 1. Measure the bias current through the current source and verify that it is approximately 4 mA. Next, ground both inputs of the amplifier and measure the voltages for V_{GSQ1} and V_{GSQ2} , the Q point values.
- (2) Set up the amplifier in differential mode as shown in Figure 2. **Make sure that the substrates (pin 4) are connected to –5 V.** Use a ramp with a range of –5 V to +5 V for v_{diff} and a frequency of 1 kHz, and observe the Voltage Transfer Characteristic of v_{o1} as a function of v_{diff} . Record several pairs of (v_{diff} , v_{o1}) voltage values (record enough values to construct a voltage transfer characteristic curve).

Caution: You must get the common-mode DC supply V_{com} up to a point where the transistors are operating properly — *i.e.*, in saturation. It is not sufficient to merely get a response at the output node. (You will get a response for V_{com} in excess of ~0.3 V above the lower supply because some current will be flowing. You will also see amplification of the differential input signal, albeit distorted.) You must get V_{com} at least up the point where your current source is operating properly — *i.e.*, at the designed 4 mA level. All your results will be invalid if this is not done properly.

- (3) Determine the differential mode gain for four different input values of v_{diff} . Use the same v_{diff} values that you used in part (7) of the pre-lab. Make two sets of measurements, one for v_{o1} and the other for v_{o2} . **Use screen capture to store results for each value of v_{diff}** to include in your lab report.

- (4) Set up the amplifier in common mode as shown in Figure 3. **Make sure that the substrates (pin 4) are connected to -5 V .** Determine the common mode gain for four different input voltage values of v_{cm} . Use the same v_{cm} values that you used in part (8) of the pre-lab. Make two sets of measurements, one for v_{o1} and the other for v_{o2} . **Use screen capture to store results** to include in your lab report. (If the output signal is noisy, try changing the oscilloscope from a normal display mode to an average display mode.)
- (5) Calculate the CMRR of the amplifier.

Results and Discussion:

- Show the calculations for the design of the current source.
- Discuss the voltage transfer characteristics and include a voltage transfer characteristic curve using values obtained in part (2) of the hardware section.
- Compare theoretical, simulation, and hardware values of differential mode and common mode gains, and explain any discrepancies.
- Explain why differential input signal amplitude should be limited to about 1 V(pp) or less. What would you expect to happen to the output signal for larger input signals?
- Attach PSPICE simulations:
 - (a) confirming current source design;
 - (b) showing the Voltage Transfer Characteristic (VTC);
 - (c) showing the differential gain of the amplifier (include curves for several different input signal amplitudes);
 - (d) showing the common-mode gain of the amplifier (include curves for several different input signal amplitudes).
- Discuss the effect of mismatched transistors by examining the gains:
 - (a) when the output is taken at v_{o1} ; and
 - (b) when the output is taken at v_{o2} .
- Discuss what could be done to improve the gain of the differential amplifier.