ES330 Laboratory Prof. S. Saraf

Lab 7: MOSFET Differential Pair with Active Load

Overview

The differential amplifier is a fundamental building block in electronic design. In this lab we will extend on the work in Lab #6, which introduced the resistively loaded differential pair. The actively loaded differential pair uses a current mirror of MOS devices that are complementary to the input pair — *i.e.*, a PMOS current mirror with an NMOS input pair, or an NMOS current mirror with a PMOS input pair.

Theory

The intrinsic stage gain A_v for an active loaded amplifier can be represented as $A_v = G_m R_o$, where G_m is the stage transconductance and R_o is the stage output resistance. A differential amplifier with active load, such as the one in Figure 1, is configured to accept a differential input signal and provide a single-ended output signal. **Note that V_{com} is a DC source, whereas v_{diff} and v_{com} are small-signal sources. In this lab exercise, either v_{diff} or v_{com} will be applied for a given measurement, but not both simultaneously**.

The equivalent stage transconductance for a differential configuration is $G_m = g_m$, or the individual transistor transconductance for either M_1 or M_2 of the input pair. The stage output resistance is $R_o = r_{o2} \| r_{o4}$, or the parallel combination of the output transistor pair (M_2 and M_4) output resistances.

The small-signal output resistance for a MOSFET operating in the saturation region is given by $r_o = 1/(l I_D)$ where l is a process technology-dependent parameter for a given channel length. Note that r_o varies inversely with the DC bias current. The value of l for each transistor can be determined by measuring the output resistance at a given bias point, as was done in Lab #4.

The common mode gain is given by Equation (1):

$$A_{cm} = \frac{v_o}{v_{cm}} = -\frac{1}{2r_{o6}} \frac{r_{04}}{(1 + g_{m3} r_{o3})} \tag{1}$$

which can be simplified to Equation (2) when $g_{m3} r_{o3} >> 1$, noting that $r_{o3} = r_{o4}$:

$$A_{cm} \cong -\frac{1}{2 g_{m3} r_{o6}}. \tag{2}$$

Pre-Lab

Assume the following device parameters:
$|V_t| = 0.7$ V, $k'_n = 25\ \mu A/V^2$ and $k'_p = 10\ \mu A/V^2$, $W/L = 100{:}1$ for both NMOS and PMOS.

- **Design** the M_5–M_6 current source for a 4 mA DC drain current in M_6 by calculating the appropriate value of R_1.

- A DC common mode voltage (V_{com}) will be required to allow bias current to flow in the complete differential amplifier circuit. **Calculate** the minimum value of V_{com} that can be applied and still ensure proper operation (*i.e.*, all transistors in saturation) of the differential pair.

- **Calculate** the expected intrinsic (let $R_L \rightarrow \infty$) small signal differential gain for the amplifier in Figure 1, where $I_{D6} = 4$ mA. The data sheet for the ALD1103 gives the output conductance at a bias point of $I_D = 10$ mA as 200 µS (µmhos) for the NMOS device and 500 µS (µmhos) for the PMOS device. These values can be used to determine r_{o2} and r_{o4}, as was done in Lab #4.

- **Calculate** the expected small-signal output resistance of the differential amplifier.

- **Develop** an expression for the CMRR of the amplifier. **Calculate** the expected common mode gain v_0/v_{com} and CMRR for the circuit in Figure 1.

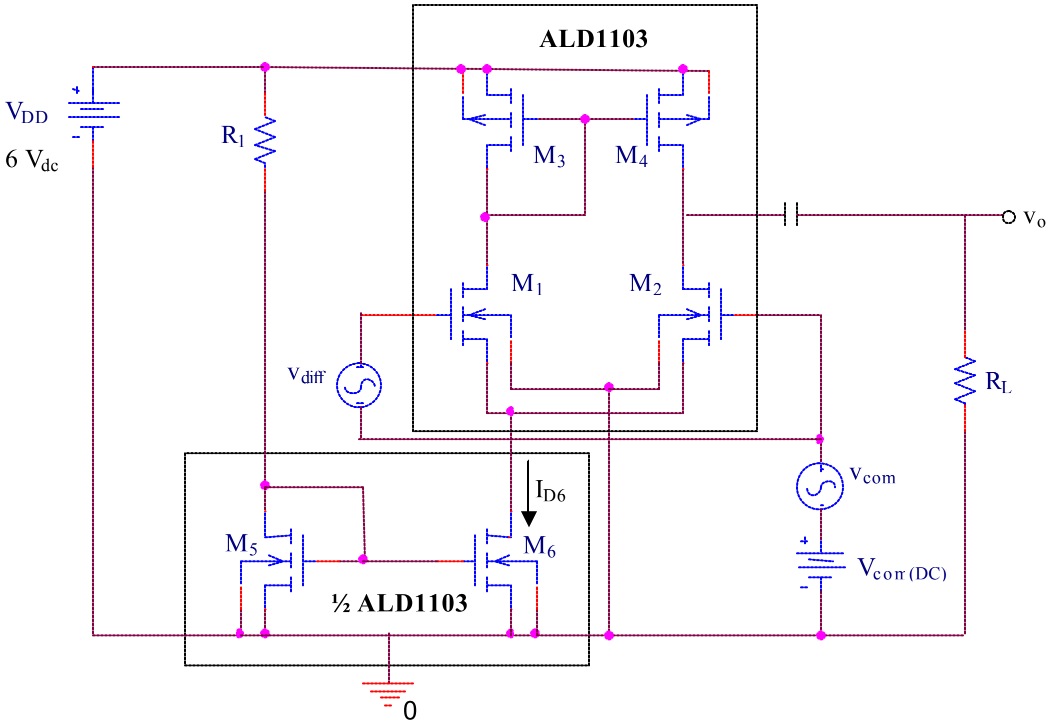


Figure 1. MOSFET Actively Loaded Differential Amplifier

Lab Exercise

Using two ALD1103 packages, build the circuit in Figure 2. The pin diagram for the ALD1103 is shown in Figure 3. **Note that all NMOS body connections (pin 4) go to the lowest supply (ground, in this case).** Since we are using a separate chip for M_1 / M_1 than we are for M_5 / M_6, we *could* eliminate body effect in M_1 and M_2 by connecting their bodies directly to their sources. However, that is not realistic because — in an integrated circuit — all the NMOS bodies are common, tied to the lowest potential in the circuit. (Also, all the PMOS substrates (bodies) are common, tied to the highest potential in the circuit.) **The substrates (pin 11) of the PMOS devices must be connected to the most positive supply voltage (V_{DD}).**

Apply power to V_{DD} before connecting the input signal. Remove the input signal before disconnecting power. Make sure you are grounded before touching the pins of the ALD1103 MOSFET package.

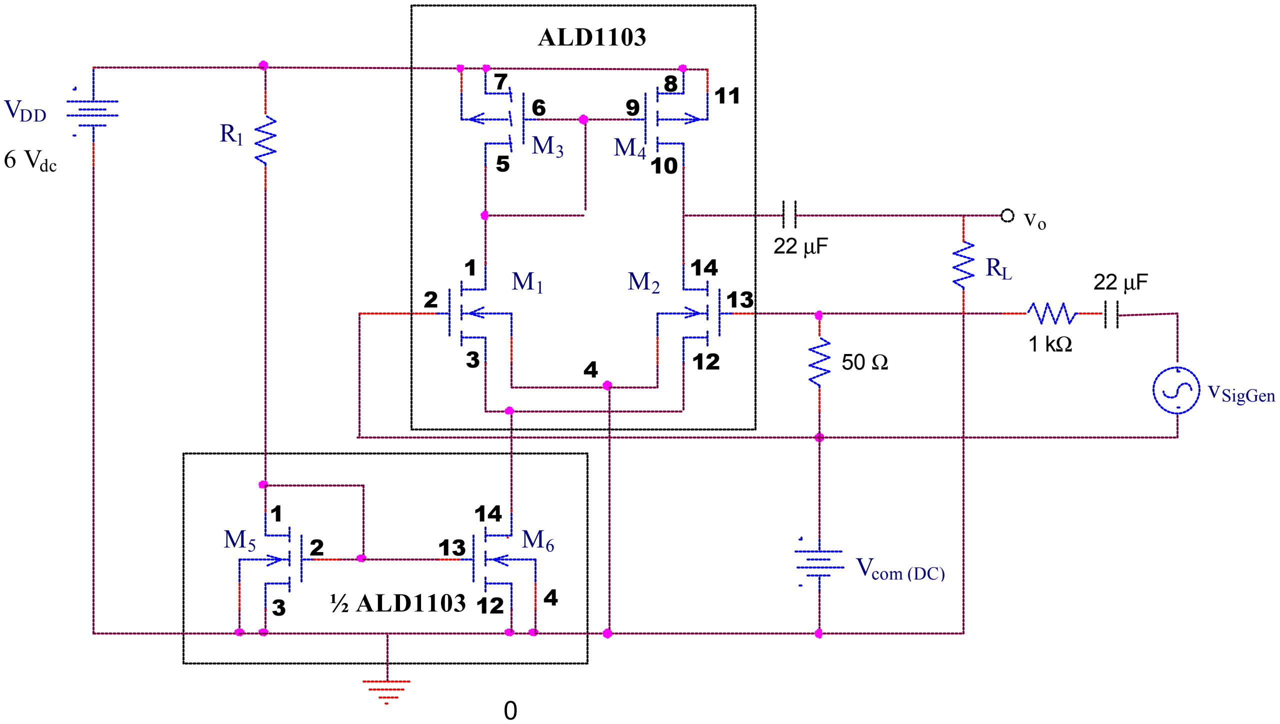


Figure 2. MOSFET Actively Loaded Differential Amplifier with Scaled Signal Generator Differential Input

1) Implement the M_5-M_6 current mirror that was designed in the pre-lab work to obtain a drain current in M_6 of 4 mA. Connect a DC power supply (the power supply's +20 V output is convenient) adjusted to 6 V DC. *Verify that the bias current in M_6 is 4 mA DC after connecting the M_6 drain to +6 V through a 1 kW resistor.* Remove the 1 kΩ resistor and connect the current mirror to the differential stage. Verify the biasing current again.

2) A small-signal differential input must be applied. Note that the signal generator connection in Figure 2 is superimposed on the DC common mode voltage supply V_{com} (use the power supply's +6 V output for V_{com}). The output of the signal generator has been scaled so that the input to the differential amplifier can be adjusted to about 10 mV. Set the signal generator to a sine wave of 100 Hz frequency and 200 mV amplitude. <u>Make sure that the signal generator is in "High–Z" mode</u>. The differential signal applied to the inputs of the differential amplifier should be verified as approximately 10 mV.

3) A common-mode DC supply must be provided in addition to the differential signal to bias the amplifier in the linear operating region (all transistors in saturation). Place a scope on the output signal node (v_o) and carefully adjust the V_{com} DC supply from zero volts until you see an <u>undistorted</u> sine wave on the display. Compare this value of V_{com} to the value calculated for pre-lab.

   <u>Caution</u>: You must get V_{com} up to a point where the transistors are operating properly — *i.e.*, in saturation. It is not sufficient to merely get a response at the output node. (You will get a response for V_{com} in excess of ~0.3 V because some current will be flowing. You will also see amplification of the differential input signal, albeit distorted.) <u>*You must get V_{com} up the point where your current source is operating properly — i.e.*, at the designed 4 mA level. All your results will be invalid if this is not done properly</u>.

4) Measure the differential mode voltage gain of the amplifier in Figure 2 for an input signal of 10 mV at 100 Hz.

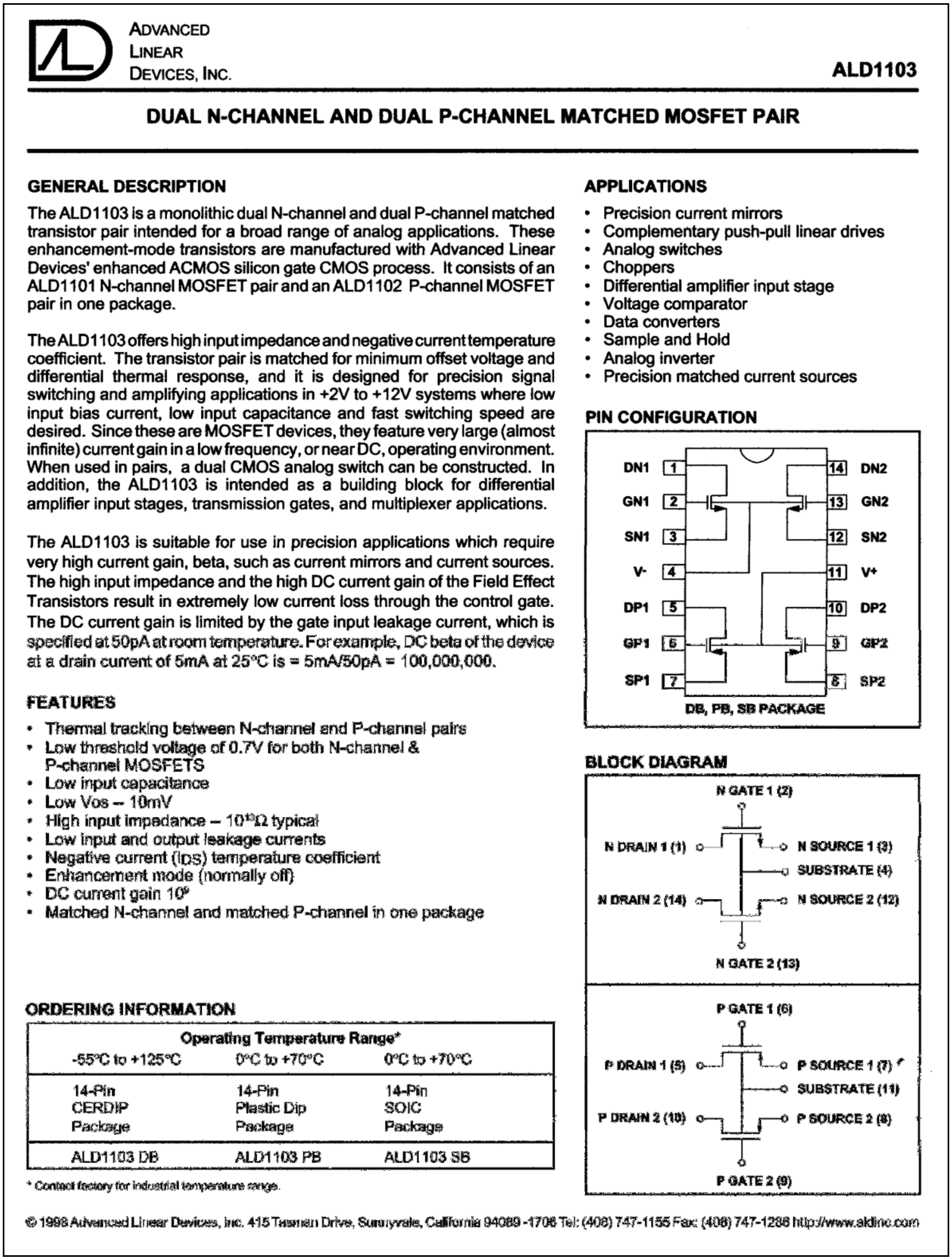
5) Maintaining the signal generator input level at 10 mV, sweep the frequency range until the output voltage drops by 3 dB. (Convert the differential gain to dB, subtract 3 dB from this value to obtain the desired 3 dB value, convert back to V/V ratio to determine the target v_o.) This determines the 3 dB bandwidth of the amplifier.

6) Part of the pre-lab work was to calculate the expected small-signal output resistance of the differential amplifier. If an equivalent resistance is ac-coupled (*i.e.*, through a capacitor) from the output node to ground, the amplitude of the signal should be reduced by a factor of ½. Verify this measurement of the small signal output resistance at 1 kHz.

7) Modify the circuit and measure the common mode voltage gain of the amplifier at a frequency of 100 Hz and at 100 kHz. (An easy way to measure common mode gain is to superimpose a large ac signal like 1 $V_{(pp)}$ on the DC offset V_{com}. (Refer to Figure 1, and let $v_{diff} = 0$.) Calculate the CMRR at 100 Hz.

Results and Discussion:

- Is the value of V_{com} obtained in Step (3) consistent with the value you calculated in your pre-lab preparations?
- What is the differential-mode voltage gain at 100 Hz?
- What is the calculated small-signal output resistance of the differential amplifier?
- When you ac-coupled a resistance that was equivalent to your calculated small-signal output resistance from the node at v_0 to ground, the amplitude of the 1 kHz signal should have been reduced by a factor of ½. Did your measurement verify this expectation?
- What is the common-mode voltage gain at 100 Hz? What is the CMRR at 100 Hz?
- Is there a significant difference in the two common-mode voltage gain values obtained in Step (7) for 100 Hz and 100 kHz? Why?
- What is the 3 dB bandwidth of the amplifier?
- How could the bandwidth of the amplifier be increased while still using the same circuit topology?
- What discrepancies have you noted in your lab measurements compared to your calculated values? How can you account for any observed differences?



ADVANCED LINEAR DEVICES, INC.

ALD1103

DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is = 5mA/50pA = 100,000,000.

FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low Vos – 10mV
- High input impedance – $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package

ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1103 DB	ALD1103 PB	ALD1103 SB

* Contact factory for industrial temperature range.

APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

PIN CONFIGURATION

BLOCK DIAGRAM

Figure 3. ALD1103 Pin-Out and Specifications