Course Description

• **CES 522: VLSI Design (3)**
  - Lecture, 3 hours. IC technology review; hardware description languages and describing hardware using one of the languages, modern VLSI design flow; circuit partitioning; clustering. Floorplanning; placement; global routing; area efficient design, area-time trade-offs. The course may require significant lab and/or project activity. Prerequisite: CES 530 or consent of instructor.

• **ES 485: Selected Topics in Engineering Science (1-3)**
  - A course on a single topic or set of related topics not ordinarily covered in the engineering science curriculum. The course may be repeated for credit as topics vary. Prerequisite: consent of instructor.
Contact

- Ryan_Hirth@yahoo.com
- Hirth@sonoma.edu

- Office hours 30 minutes before and after class or by prior arrangement.
Text books

• "Digital Design A Systems Approach" by William J. Dally and R. Curtis Harting.

• “SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling” by Simon Davidmann, Peter Flake, Stuart Sutherland

• “SystemVerilog for Verification: A Guide to Learning the Testbench Language Features” by Chris Spear, Greg Tumbush
Syllabus

Week #1 (Jan 25,27): Introduction, review of Logic Fundamentals, Verilog/system verilog, standard cell process

Week #2(Feb 1,3): Basic logic design, combinational and sequential logic

Week #3(Feb 8,10): State machines, FIFO, pipelines

Week #4 (Feb 15,17): Quiz, DV environment, testcases

Week #5 (Feb 22,24): Serial interfaces, CMOS IOs

Week #6 (Feb 29, Mar 2): Processors, busses, IP integration : SRAM Memory

Week #7 (Mar 7,9): Quiz, Algorithms, scheduling, arbitration, searching , Debug – lab, sim, test interfaces

Week #8 (Mar 14,16): Spring Break

Week #9 (Mar 21,23): External memory : DRAM interfaces

Week #10 (Mar 28,30): Signal processing, Arithmetic operations

Week #11(Apr 4,6): review, midterm(6th)

Week #12(Apr 11,13): CRCs, Error correction

Week #13(Apr 18,20): STA, DFT – jtag, atpg, functional

Week #14(Apr 25,27) : Physical design/FPGA/ clocks and reset/ PLLs/ floorplanning/ P&G

Week #15(May 2,4): Synthesis and P&R

Week #16(May 9,11): Review

May 16: Final  5pm-6:50pm (http://www.sonoma.edu/academics/pdf/2016/16spring_finals.pdf)