



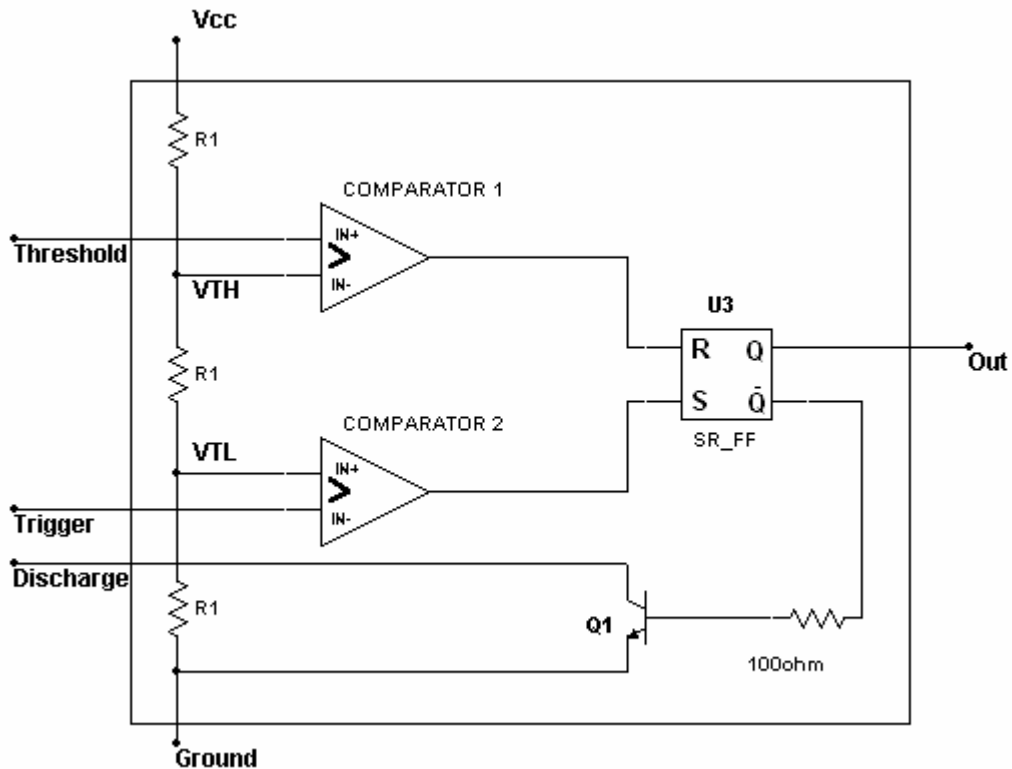
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THE 555 IC TIMER

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THE 555 IC TIMER



Block diagram representation of the 555 timer circuit.

The circuit consists of two comparators, an SR flip-flop and a transistor Q1 that operates as a switch. One power supply is (V_{cc}) is required for operation, with the supply voltage typically 5V. A resistive voltage divider, consisting of the three equal-valued resistors labeled R1, is connected across V_{cc} and establishes the reference (threshold) voltages for the two comparators.

These are $V_{TH} = 2/3 V_{cc}$ for comparator 1 and $V_{TL} = 1/3 V_{cc}$ for comparator 2.

Characteristics of Type S-R Flip-Flop

S	R	Q	Q'	
0	0	Q	Q'	No change
0	1	0	1	Reset State
1	0	1	0	Set State
0	0	?		Unpredictable

Monostable Multivibrator Using The 555 IC

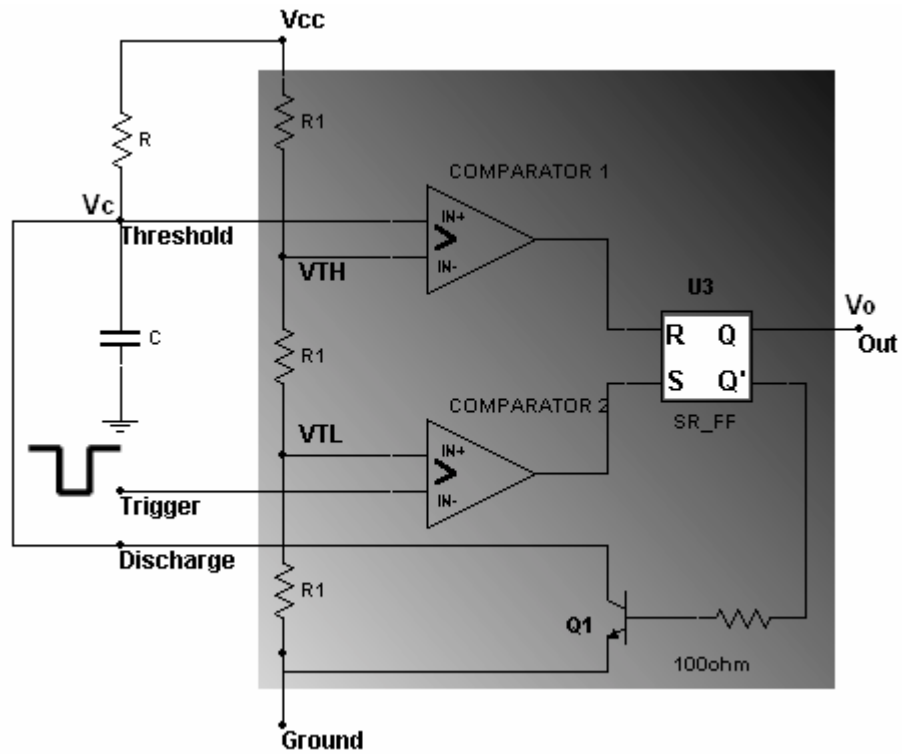
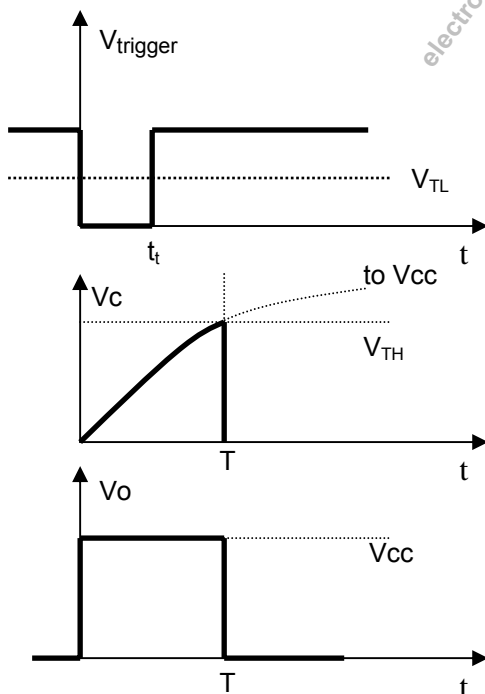


Figure above shows a monostable multivibrator implemented using the 555 IC together with an external resistor R and an external capacitor C.



S	R	Q	Q'	
0	0	Q	Q'	No change
0	1	0	1	Reset State
1	0	1	0	Set State
0	0	?		Unpredictable

1-Initial State :S=0 R=0 $V_{\text{Trigger}} > V_{\text{TL}}$

Initially, Because $V_c=0V$ and $V_{\text{TH}} = 2/3V_{\text{cc}}$ and so $V_{\text{TH}} > V_c$ the output of the comparator 1 is 0V that is $R=0V$ (R =flip-flop input). Again because $V_{\text{TL}}=1/3V_{\text{cc}}$ and $V_{\text{trigger}} > V_{\text{TL}}$ the output of the comparator 2 is 0V that is $S=0V$ (S =flip-flop input). When R & S is equal to 0V there will be no change at the outputs of the flip-flop. Assuming the initial output of flip-flop for $Q=0V$ (that is V_o) and so $Q'=1V$ (that is transistor bias voltage).

In the stable state that is V_o is equal to 0 ($Q=0$) thus its Q' output will be high, turning on transistor Q_1 . Transistor Q_1 will be saturated, and thus V_c will be close to 0V. Current coming from R will not charge C because current choose the short-circuited way that is current flows to the ground thru saturated transistor Q_1 . Look at the figure for step 1.

2- Triggered signal applied, V_{trigger} falls down below V_{TL} . $V_{\text{Trigger}} < V_{\text{TL}}$ $S=1$ $R=0$, $Q=1$ $Q'=0$

To trigger the monostable multivibrator, a pulse signal smaller than V_{TL} is applied. As V_{trigger} goes below V_{TL} , the output of the comparator 2 goes to the high level thus setting the flip-flop as $S=1$ $R=0$ for a short-time (it depends on pulse duration). For $S=1$ and $R=0$ from the table the $Q(V_o)$ will be high (V_{cc}) and Q' will be low (0V). $Q'=0V$ will cause the **transistor Q_1 to be off**. Then current will flow into the capacitor and it will **charge the capacitor**. Explanation will continue in step 4.

Trigger signal makes $S=1$ for a short time, therefore capacitor begins to charge

3- V_{trigger} rises up above V_{TL} $S=0$ $R=0$, $Q=1$ $Q'=0$ (no change)

The value of trigger signal below V_{TL} lasts for a short time. It rises up again above V_{TL} . Then the output of the comparator 2 will be again low (0V) and so $S=0$ and $R=0$ that means flip-flop **will not change its state** ($Q=1$ $Q'=0$) so capacitor continue to charge.

Trigger signal returns its stable state that makes $S=0$, capacitor continues to charge because $S=0$ and $R=0$ is no change state outputs of flip-flop remains same

4- Capacitor can charge up to V_{TH} $S=0$ $R=1$, $Q=0$ $Q'=1$

During charging when capacitor voltage (V_c) reaches $V_{\text{TH}}=2/3V_{\text{cc}}$ output of the comparator 1 changes its state and the output of the **comparator 1 will be high**. Note that S is **not** equal to 1 because trigger signal rises up to its stable state (above V_{TH}) quickly. S is equal to 1 only for a short time and this is enough for to start the charging of the capacitor.

If the duration of the trigger signal below V_{TL} lasts more than the duration the capacitor to be charged up to V_{TH} then S and R will be equal to 1 and that will result in unpredictable output of the flip-flops.

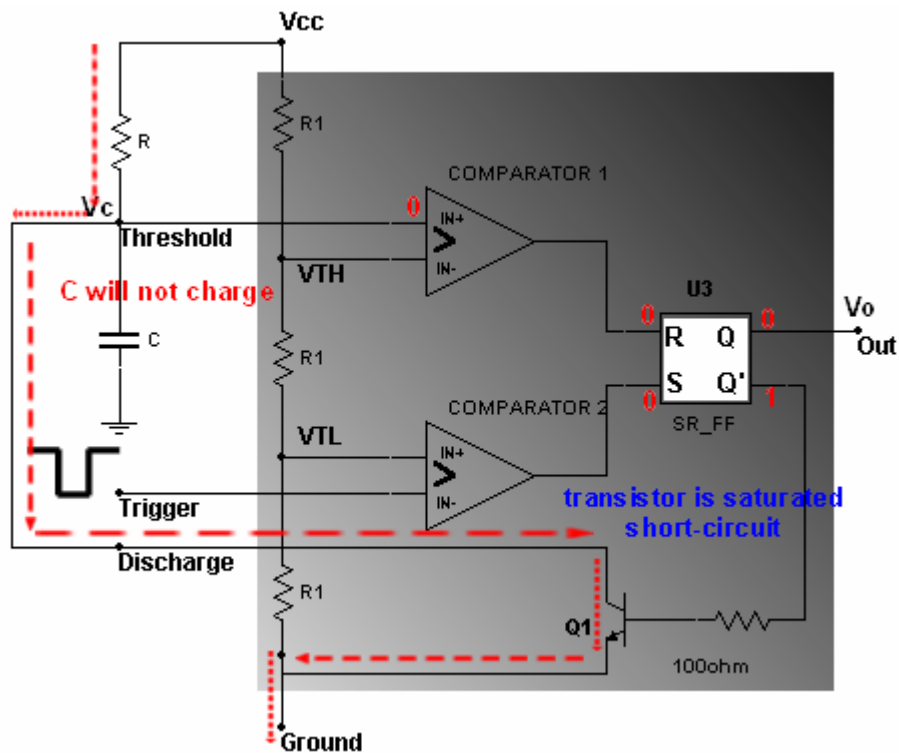
Now $S=0$ and $R=1$ that means $Q=0(V_o)$ and $Q'=1$. Transistor will be saturated again when $Q'=1$ and so capacitor will **discharge quickly** thru the saturated transistor (Note that it will discharge very quickly because the resistance of the short-circuited way is approximately zero).

5- Capacitor discharges quickly $S=0$ $R=0$, $Q=0$ $Q'=1$ (no change)

Because the saturated transistor discharging the capacitor, the output of the comparator 1 will be again low (0V). Now $S=0$ and $R=0$ that means the output of the states will remain same and $Q(V_o)$ is equal to zero.

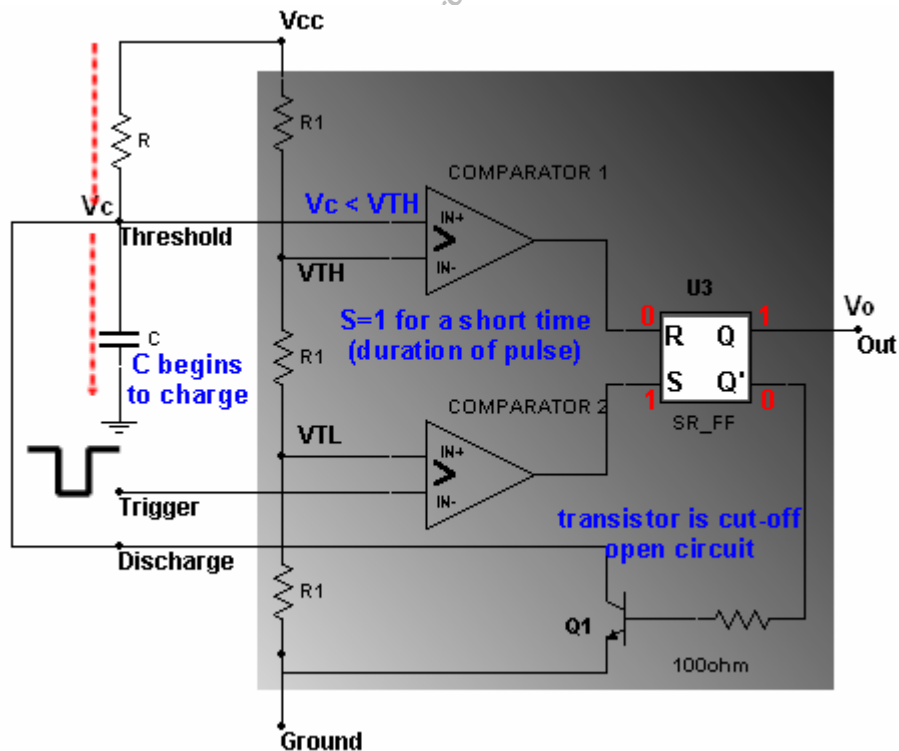
This happenings will occur again until a new trigger signal is applied.

Figure for STEP-1



C will not charge current flows thru transistor, short-circuit way.

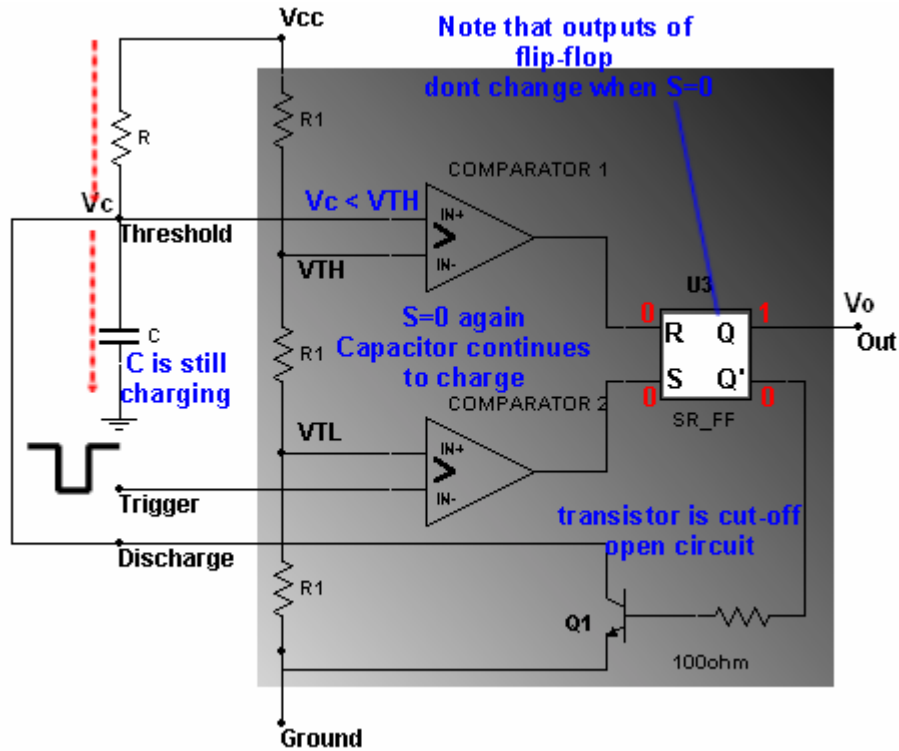
Figure for STEP-2



Capacitor continues to charge when trigger signal is applied.

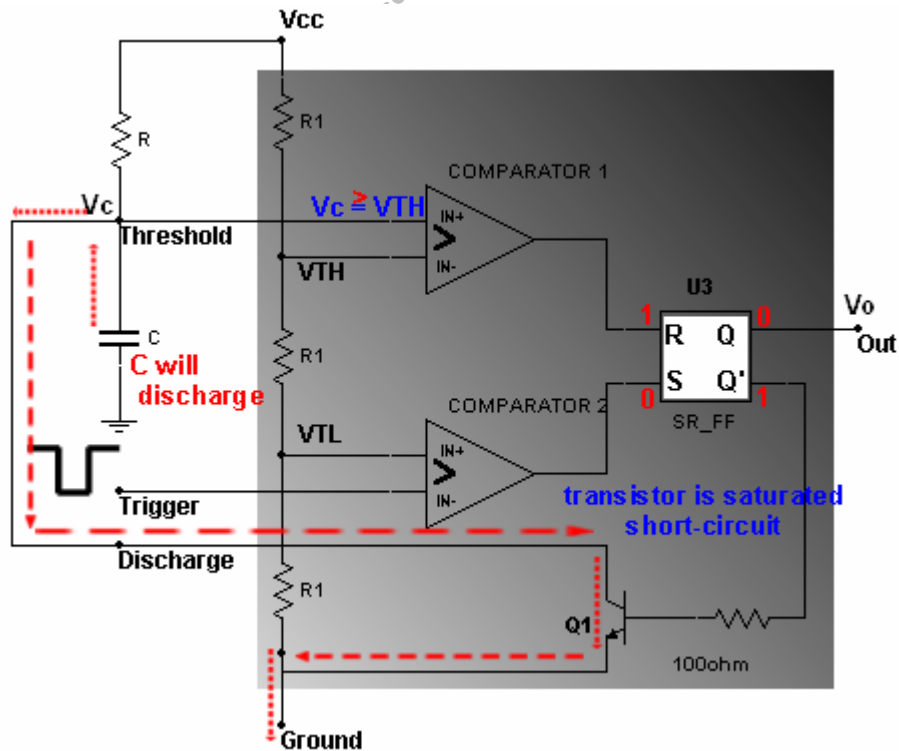
Trigger signal makes $S=1$ for a short time, therefore capacitor begins to charge

Figure for STEP-3



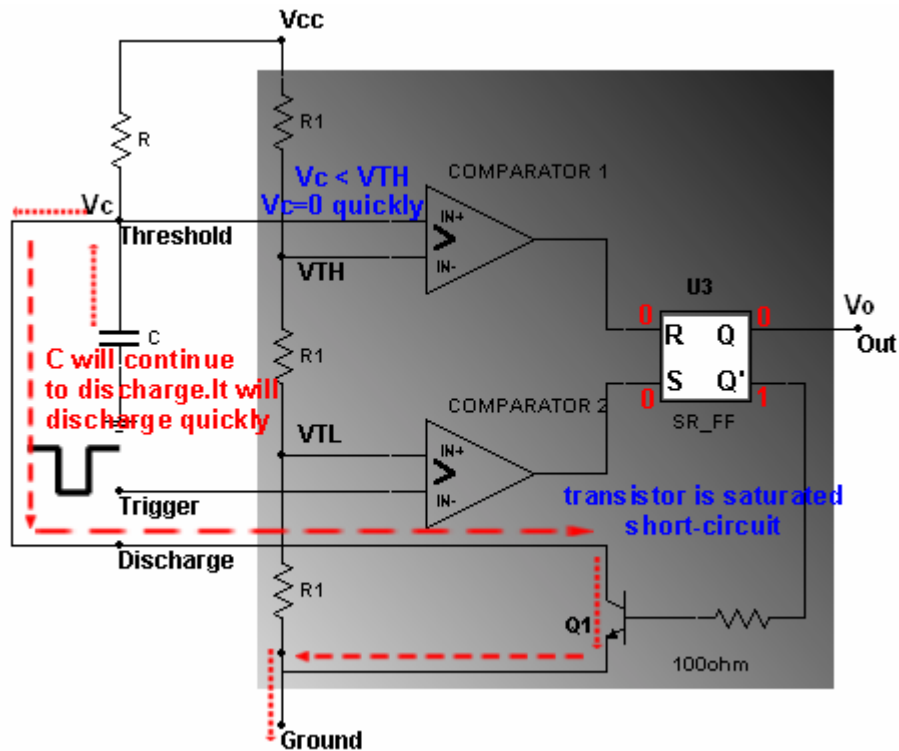
S=1 makes Q=1 Q'=0 and S returns to 0 quickly. This will not affect the outputs of the flip-flop (no change state). Capacitor continues to charge.

Figure for STEP-4



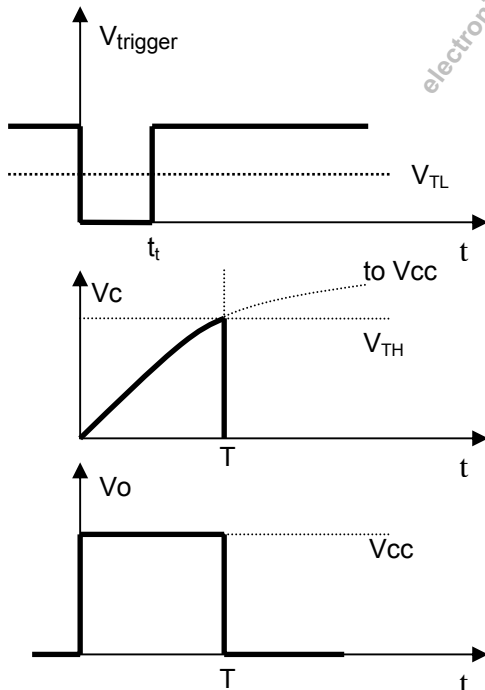
When capacitor charges up to V_{TH} , output of the comparator 1 will be high and so R=1 S=0 → Q=0 Q'=1 This will cause transistor to be saturated and capacitor will discharge through the transistor as it is indicated.

Figure for STEP-5



Capacitor will discharge quickly and $V_{TH} > V_C$ so R=0 and S=0. This happens again if a new trigger pulse signal is applied.

CALCULATION OF THE WIDTH OF THE OUTPUT PULSE :



V_c can be expressed as:

$$V_c = V_{cc}(1 - e^{-t/RC})$$

Substituting $V_c = V_{TH} = 2/3 V_{cc}$ at $t = T$ gives:

$$\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-T/RC})$$

$$e^{-T/RC} = 1 - \frac{2}{3}$$

$$e^{-T/RC} = \frac{1}{3}$$

$$T = RC \cdot \ln 3$$

$$T \cong RC \cdot 1.1$$

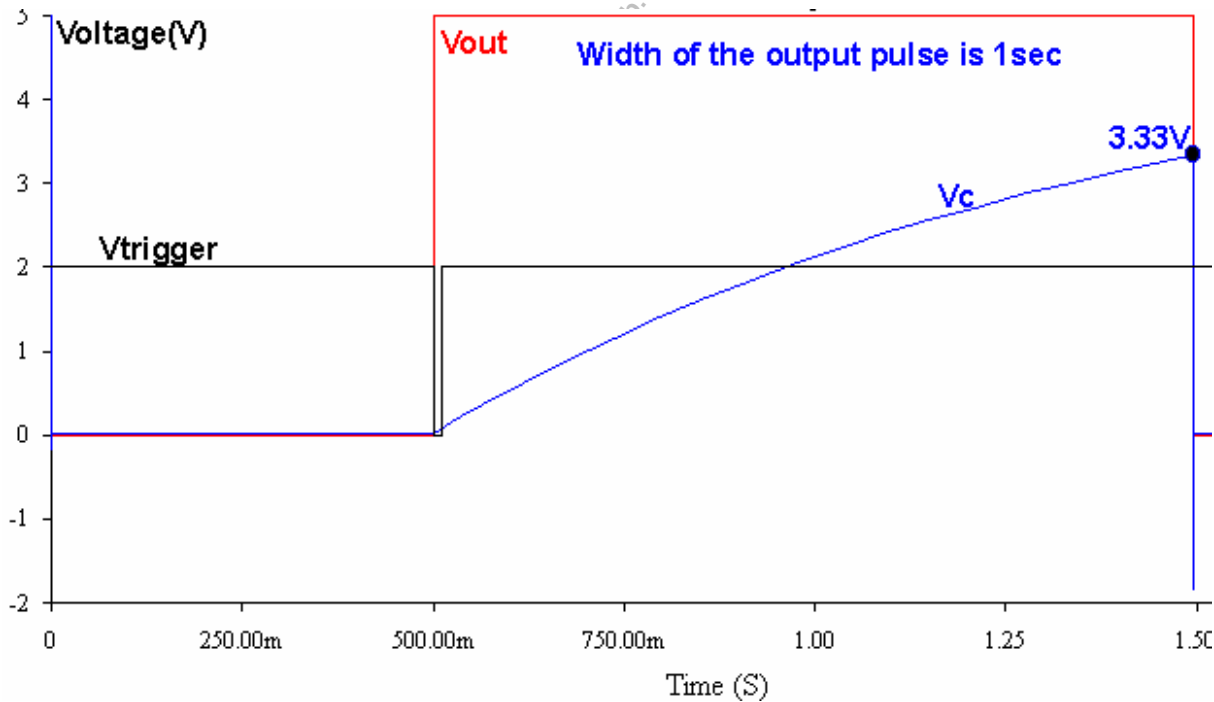
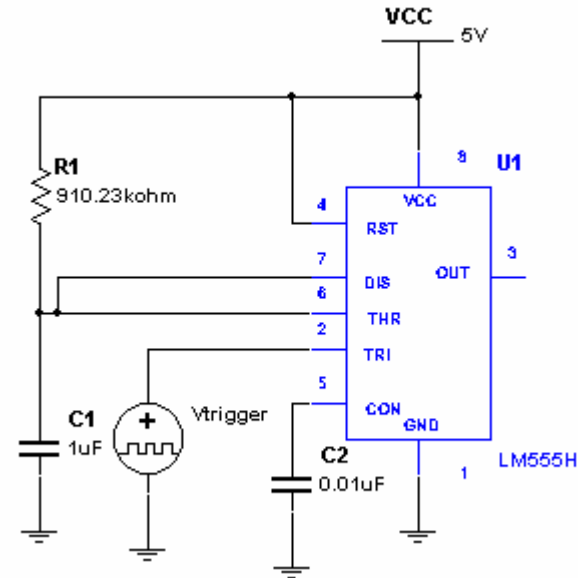
EXAMPLE 1: Using a 1uF capacitor C , find the value of R that yields an output pulse of 1 second in the monostable circuit of 555 IC.

SOLUTION:

$$T = RC \cdot \ln 3$$

$$1s = (R) \cdot (1\mu F) \cdot \ln 3$$

$$R = 910.23K\Omega$$



Note that pulse width of the $V_{trigger}$ is smaller than pulse width of the output signal.
 $3.33V = V_{TH} = (2/3) \cdot V_{CC} (V_{CC}=5V)$

Control Voltage:

By imposing a voltage at control voltage pin, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage-controlled oscillator, pulse-width modulator, etc. For applications where the control it is **strongly recommended that a bypass capacitor** (0.01uF) be placed across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Limits for external components:

Manufacturers' datasheet will help us to determine limit value of external components. For example determining R in monostable circuit can be calculated as:

$$R_{\max} = \frac{V_{CC} - V_{CAPACITOR}}{I_{THRESHOLD}} \quad I_{THRESHOLD} \text{ can be obtained from manufacturer's datasheet.}$$

For NE555 $I_{THRESHOLD}$ is 0.25uA

$V_{CAPACITOR}$ is equal to $2/3V_{CC}$ for monostable circuit of 555

$$R_{\max} = (5V - 3.33V)/0.25\mu A \quad \mathbf{R_{\max} = 6.68M\Omega}$$

Note that if using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

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Astable Multivibrator Using the 555 IC

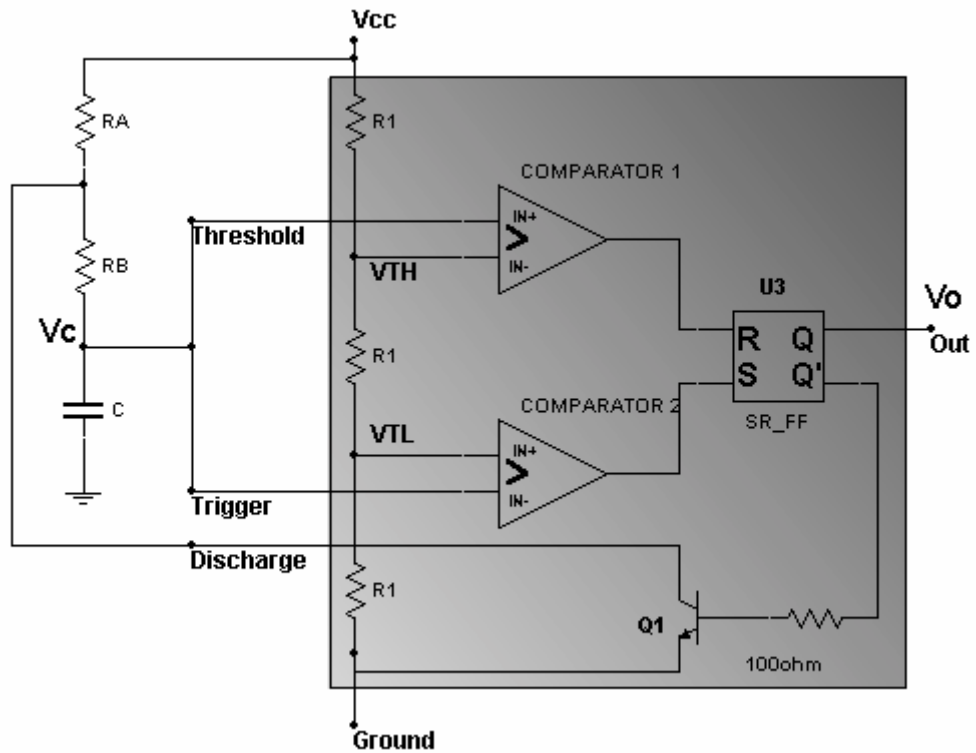
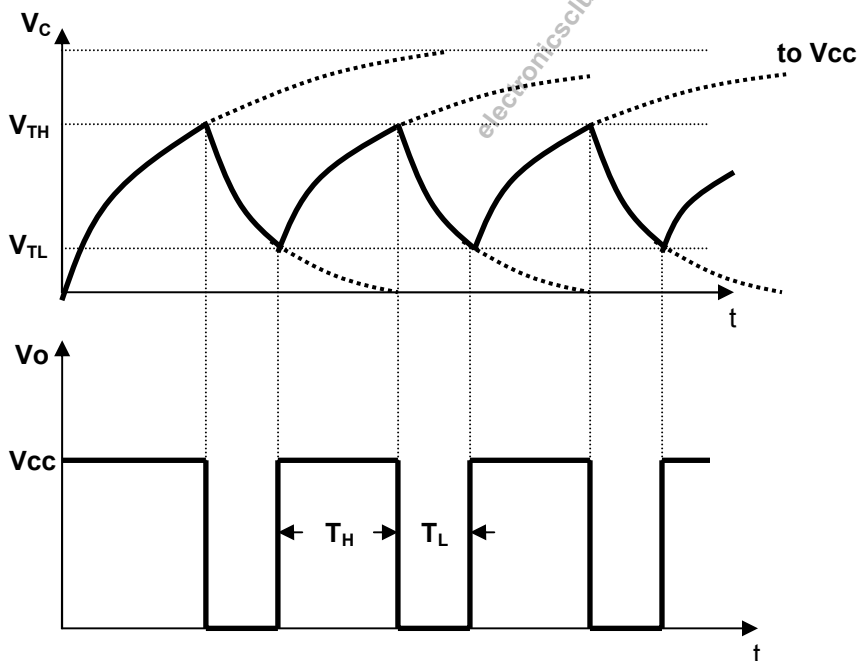


Figure above shows an astable multivibrator implemented using the 555 IC together with an external resistor R_A , R_B and an external capacitor C.



1-Initial State $S=1 R=0 \rightarrow Q=1 Q'=0$ (C begins to charge)

Initially capacitor is discharged or empty. At this time $V_{TH} > V_C$ causes output of the comparator 1 to be 0 so $R=0$ and $V_{TL} > V_C$ causes output of the comparator 2 to be 1 so $S=1$.

For $S=1$ and $R=0$, $Q=1$ (high, V_{CC}) and $Q'=0$ (low, $0V$). Thus **V_o is high and transistor is OFF.**

Capacitor C will charge up through the series combination of R_A and R_B , and the voltage across it, V_C , will rise exponentially toward V_{CC} .

2- $V_C \geq V_{TL}$, comparator 2 \rightarrow Low $S=0 R=0 \rightarrow Q=1 Q'=0$ (no change, C is still charging)

As V_C crosses the level equal to V_{TL} , the output of the comparator 2 goes low. ($V_C \geq V_{TL}$, comparator 2 \rightarrow Low). This however has no effect on the circuit operation because this will make the inputs of the flip-flop as $S=0$ and $R=0$ (no change state) which means outputs of flip-flop will **remain same**.

This state continues until V_C reaches and begins to exceed the threshold of comparator 1, V_{TH} .

3- $V_C \geq V_{TH}$, comparator 1 \rightarrow High $S=0 R=1 \rightarrow Q=0 Q'=1$ (C begins to discharge)

When V_C reaches and begins to exceed V_{TH} , the output of the comparator 1 goes **high** and **resets** the flip flop ($S=0 R=1 \rightarrow Q=0 Q'=1$). Thus **V_o goes low**, Q' goes **high** and so transistor is turned **ON**.

The saturated transistor causes a voltage of approximately $0V$ to appear at the common node of R_A and R_B . Thus C begins to **discharge** thru R_B and the collector of the transistor.

Note that $R = 1$ (flip-flop input) for a very short time.

4- $V_C \leq V_{TH}$, comparator 1 \rightarrow Low $S=0 R=0 \rightarrow Q=0 Q'=1$ (no change, C continues to discharge)

V_C will drop again below V_{TH} **immediately** after discharging process is started. $S=0$ and $R=0$ will not affect the system (no change state)

The voltage V_C decreases exponentially with a time constant $R_B \cdot C$ toward $0V$. This state will continue until V_C reaches V_{TL} .

5- $V_C \leq V_{TL}$, comparator 2 \rightarrow High $S=1 R=0 \rightarrow Q=1 Q'=0$ (C begins to charge)

When V_C reaches the threshold of comparator 2, V_{TL} , the output of comparator 2 goes high and then $S=1 R=0$ causes $Q=1$ and $Q'=0$. Thus output **V_o goes high** and Q' goes low, **turning off the transistor**.

Capacitor C begins to charge through the series equivalent of R_A and R_B , and its voltage rises exponentially toward V_{CC} with a time constant $(R_A + R_B) \cdot C$. This rise continues until V_C reaches V_{TH} , at which time the output of comparator 1 goes high, resetting the flip-flop, and the cycle goes on.

Determining the Period $T = T_H + T_L$:

For T_H :

From the general solution for step and natural responses :

$$X(t) = X_F + [X(t_0) - X_F] \cdot e^{-(t-t_0)/\tau}$$

$$V_C = V_{CC} + [V_{TL} - V_{CC}]e^{-t/\tau}$$

or ;

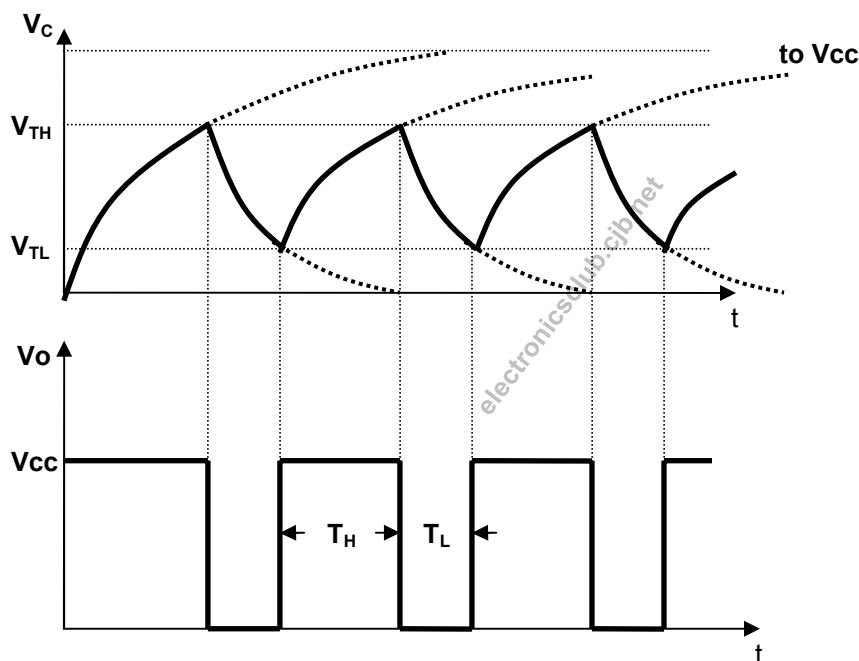
$$V_C = (\text{Final Val} - \text{Initial Val}) (1 - e^{-t/RC}) + \text{shifting}$$

$$V_C = (b-a) (1 - e^{-t/RC}) + a$$

$$V_C = (V_{CC} - V_{TL})(1 - e^{-t/\tau}) + V_{TL}$$

Note that :

$$V_C = (V_{CC} - V_{TL})(1 - e^{-t/\tau}) + V_{TL} \text{ is equal to } V_C = V_{CC} + [V_{TL} - V_{CC}]e^{-t/\tau} \text{ where } \tau = (R_A + R_B) \cdot C$$



Substituting $t=T_H$ $V_C=V_{TH}=2/3V_{CC}$ and $V_{TL}=1/3V_{CC}$ in the equation $V_C = (V_{CC} - V_{TL})(1 - e^{-t/\tau}) + V_{TL}$

$$\frac{2}{3}V_{CC} = (V_{CC} - \frac{1}{3}V_{CC})(1 - e^{-t/\tau}) + \frac{1}{3}V_{CC} \quad \text{where } \tau = (R_A + R_B) \cdot C$$

$$e^{-t/\tau} = \frac{1}{2}$$

$$T_H = (R_A + R_B) \cdot (C) \cdot (\ln 2)$$

$$T_H = 0.69(C)(R_A + R_B)$$

For T_L :

$$X(t) = X_F + [X(t_0) - X_F] \cdot e^{-(t-t_0)/\tau}$$

$$V_C = 0V + [V_{TH} - 0]e^{-t/\tau}$$

$$V_C = V_{TH} \cdot e^{-t/\tau}$$

$$\text{where } \tau = R_B \cdot C$$

For $t=T_L$ $V_C=V_{TL}=1/3V_{CC}$ and $V_{TH}=2/3V_{CC}$

$$V_C = V_{TH} \cdot e^{-t/\tau} \quad \text{where } \tau = R_B \cdot C$$

$$1/3V_{CC} = 2/3V_{CC} \cdot e^{-t/\tau}$$

$$T_L = R_B \cdot C \cdot \ln 2$$

$$T_L = 0.69 R_B \cdot C$$

$$T = T_H + T_L$$

$$T = 0.69(C)(R_A + R_B) + 0.69 R_B \cdot C$$

$$T = 0.69 \cdot C \cdot (R_A + 2R_B)$$

Also the **duty cycle** of the output square wave can be found as:

$$DutyCycle = \frac{T_H}{T_H + T_L} = \frac{R_A + R_B}{R_A + 2R_B}$$

Note that the duty cycle will always be greater than 0.5(50%). It approaches to 0.5 if R_A is selected much smaller than R_B .

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